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Gennadiy G. Bortnyk, Vasyl M. Kychak, Mikola V. Vasylkivskyi, Bogdan Pinaiev, Ryszard S. Romaniuk, Gayni Karnakova, "The method of improving the dynamic range of jitter analyzers in optical-fiber transmission systems," Proc. SPIE 10808, Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments 2018, 108080K (1 October 2018); doi: 10.1117/12.2501499

Event: Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments 2018, 2018, Wilga, Poland

The method of improving the dynamic range of jitter analyzers in optical-fiber transmission systems

Gennadiy G. Bortnyk*[a], Vasyl M. Kychak[a], Mikola V. Vasylkivskyi[a], Bogdan Pinaiev[a],
Ryszard S. Romaniuk[b], Gayni Karnakova[c]
[a]Vinnytsia National Technical University, Vinnytsia, Ukraine; [b]Warsaw University of Technology,
Warsaw, Poland; [c]Taraz State University after M. Kh. Dulaty, Taraz, Kazakhstan

ABSTRACT

The method of improving the dynamic range of analog-to-digital conversion path of jitter analyzers in optical-fiber transmission systems in the conditions of dispersion distortions of optical signals is suggested in the work. The impact of the clock frequency jitter of an analog-to-digital converter on the noise features of the analog-to-digital conversion path by paralleling the process of the analog-to-digital conversion of signals with the correction of clock frequency jitter has been analyzed.

Keywords: dynamic range, jitter, analyzer, fiber optics transmission systems

1. INTRODUCTION

The speed increase of data flows is caused by a greater number of the tasks which are solved with the help of data communication networks. The advanced data communication networks are designed on the basis of fiber-optical transmission systems (FOTS). The rapid application of transfer technologies based on fiber optics enhances the requirements for synchronization in FOTS. An important criterion for synchronization signals quality in FOTS is data dependent jitter (DDJ). It should be mentioned that the accumulation of data signals jitter in consequence of dispersion distortions in digital line channels lowers spectral and energy effectiveness of FOTS[1].

High speed FOTS are featured with high requirements to the stability of optic signals processing channels. Therefore, to control their functioning, it is necessary to apply digital signals analyzers which provide accurate determination of jitter in a wide dynamic range[2]. The main factor to determine the effectiveness of phase jitter (PJ) estimation is the functioning quality of jitter signal processing channel. The jitter parameters may gain the values found in a wide dynamic range. Thus, the main requirement, set to the jitter analyzer, is a low level of its PJ. Modern PJ analyzers are characterized with self-jitter which equals 0.05 UI and more. Such values of self-jitter do not make it possible to fulfill the PJ analysis in FOTS with frequency-dependent sensitivity according to the main parameter on the level of 0.01 UI[1].

2. PUBLICATIONS ANALYSIS

Phase jitter self-level causes a great impact on the jitter analysis results. The problem is that the analyzer self-jitter and the determined PJ of FOTS interact according to complicated laws depending on the form and the phase of a signal. The present level of PJ analyzers does not make it possible to design jitter estimation devices with the self-jitter parameters approaching to the values of 0 UI, that's why the analyzer self-jitter has a permanent impact on the final results of quality analysis of FOTS[3,4]. To compensate self-induced PJ, some manufacturers use software procedures in data processing[5]. Such a method is ineffective as under study PJ depends not only on analyzer hardware, but also on the structure of under study stream and signal structure. Consequently, the method of software compensation causes serious jitter estimation errors in FOTS.

Hereby, the only method to gain a wide range of PJ estimation is high performance of the analyzer with low level of self-induced PJ. This is the main reason why the PJ analysis greatly complicates the hardware. Thus, the realization of jitter analyzers with wide dynamic range is practically impossible.

*bgen88@gmail.com

Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments 2018,
edited by Ryszard S. Romaniuk, Maciej Linczuk, Proc. of SPIE Vol. 10808, 108080K
· doi: 10.1117/12.2501499

One of the main stages of jitter signal processing U_{Tj}, which is formed on the output of phase detector (PD), is its analog-to-digital conversion (Fig. 1.) or a set of digits. The parts of ADCP, namely: selection and save unit (SSU), discretization impulses generator f_S (DIG), quantizer (QT) and encoder (ED) characterize the PJ estimation device in whole[6]. Real ADCP put forward essential distortions and obstacles in digital PJ signal $x(n)$ presentation in the form of parasitic spectrum components and noises resulting from nonlinearity and instability of functional elements, characteristic and induced noises, as well as parasitic signals[6].

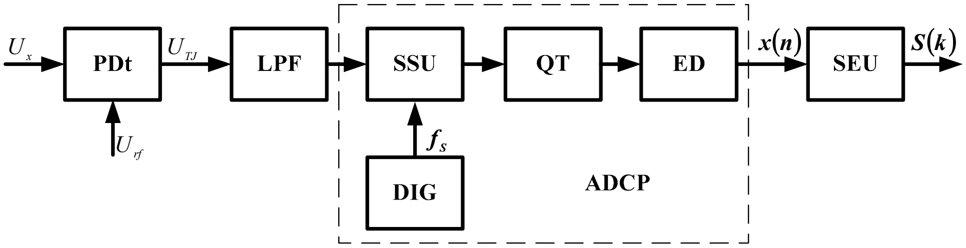

Figure 1. Generalized structure of PJ estimation device.

The expansion of dynamic range of jitter analyzer based on the units of signals digital processing is provided by higher bitness of digital means. At the present stage of circuitry improvement such an increase creates no difficulties. As for the ADCP, on the one hand, the distortions which are included at the analog-to-binary conversion cannot be usually eliminated at following processing, but on the other hand the dynamic range extension of analog-to-digital converter (ADC) is a quite complicated task. Thus, to gain high performance of PJ estimation means it is necessary first to solve the problem of dynamic range extension of ADCP of jitter analyzers.

3. RESEARCH OBJECTIVES AND TASKS

The aim of the work is the dynamic range extension of analog-to-digital conversion path of jitter analyzers in FOTS. To attain the given aim, the following tasks have to be solved:

- to analyse the impact of clock frequency jitter of ADC on the dynamic range of ADCP of PJ signal;
- to develop the method of the paralleling of the process of analog-to-digital conversion of jitter signals with the correction of discretization pulses delays;
- to analyse the effectiveness of the given method of analog-to-digital conversion with the correction of clock frequency jitter.

4. RESULTS

The main conformity to discretization and quantization processes of PJ signals is that due to the end time of one conversion and the indeterminateness of its time-off it is impossible to reach the single-valued correspondence between the counting-outs values and the points of time. Using several ADC microchips in ADCP of PJ signals, the differences in aperture delays between the converters are observed. An essential aperture error appears in case of variation of aperture delay in different discretization cycles. It should be mentioned, that the effects of phase jitter of discretization clock pulses cause the errors of the same type[7,8].

The impact of the aperture jitter and the discretization clock pulses on the dynamic range of ADCP is to be analyzed. Taking into account, that the root-mean-square value of complete scale of conversion equals $U_m/\sqrt{2}$, then it is possible to find the dynamic range:

$$D_a = 20\lg\left[\frac{U_m/\sqrt{2}}{\Delta U_{rms}}\right] = 20\lg\left[\frac{1}{2\pi f\Delta\tau_a}\right]. \qquad (1)$$

The dependency of the dynamic range on the frequency of the input sinusoidal signal (Fig. 2.) can be defined on the basis of the expression (1). The derived dependencies fit an ideal frequency-dependent sensitivity of ADC without regard for the quantization noises, that is, the main factor which impacts the dynamic range is the input counting-offs jitter due to the aperture indeterminateness and the instability of pulses fronts of the discretization. It is depicted in the graphs that the dynamic range narrows with the increase of the input signal frequency and the aperture jitter.

Thus, jitter signal discretization with the help of ADC with high values of aperture jitter results $\Delta\tau_a$ in considerable discrepancy between operation speed of ADC and discretization period. The discrepancy obtains 2÷3 orders and complicates the process of analog-to-digital conversion because even for low frequency PJ signals, high-performance ADC are required. To gain high operating speed of analog-to-digital conversion of path of PJ signal, structural construction is suggested which is based on the principal of processing channels parallelization with time-based sweep. Such ADC can function with the speed exceeding the operating speed of some microchips of ADC. But this construction principal of ADCP is featured with narrow dynamic range. The narrowing of dynamic range is caused by the appearance of aperture defect in some models of ADC and fronts instability of discretization impulses.

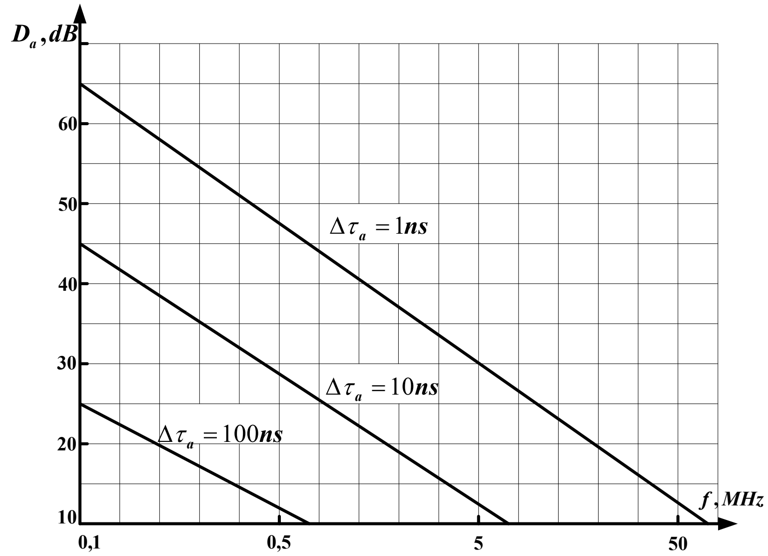

Figure 2. The dependencies of the dynamic range, conditioned by the counting-offs jitter, on the input signal frequency.

In this case, the conversion of analog signal into digital code is implemented with the help of L in-parallel modules ADC1÷ADC L. Discretization sum frequency for the process equals f_S. Discretization impulses are sent to strobe inputs of modules of ADC with the frequency f_s/L. Besides, for two in-series ADC with the help of delay units (DU), the phase shift between impulses fronts equals $1/f_s$.

At the best, if all the ADC modules have the same dynamic parameters and ADCP is featured with low level of aperture defect as well as discretization impulses jitter, then parallel structure of analog-to-digital conversion, as well as some ADC modules, obtain the same discretization frequency and digit capacity. But in consequence of nonidentity of aperture time in every ADC modules and the problem of appropriate delay maintenance between convertors modules, the dynamic range of a parallel ADC appears to be much narrower than in basic structures.

According to DSP theory the frequency spectrum of the sinusoidal signal on the output of flash ADCs equals[9,10]:

$$X(f)=\frac{1}{T_S}\sum_{k=-\infty}^{\infty}A(k)\cdot\delta\left[f-f_{in}-k\left(\frac{4\pi^2}{LT_S}\right)\right], \qquad (2)$$

where: $T_s=1/f_s$ – sampling (discretization) period of ADC; $A(k)$ values of the spectrum components; f_{in} input sinusoidal signal frequency of ADC; $\delta[x]=0$, if $x \neq 0$; $\delta[x]=1$, if $x=0$.

Let the aperture shift and the impulses discretization instability are estimated with the value of differential phase instability:weights:

$$m_l = \frac{\Delta\tau_a - \Delta\tau_{al}}{\Delta\tau_a}, \tag{3}$$

where: $\Delta\tau_a$ – nominal value of phase shift of ADC; $\Delta\tau_{al}$ – phase shift of ADC module.

Applying discrete Fourier transform (DFT) in consideration of (3), the value of frequency component of spectrum can be defined:

$$A(k) = \sum_{l=0}^{L-1}\left[\frac{1}{L}\cdot e^{-j2\pi\cdot m_l \frac{f_{in}}{f_S}}\right]\cdot e^{-jk\cdot l\left(\frac{2\pi}{L}\right)}. \tag{4}$$

The derived expression states that digital spectrum of input signal of parallel ADC has L pairs of frequency components which are equally spaced on the frequency axis. And the center of one pair is at the distance T_S/L to the center of the following pair of components. The number of spectrum components pairs on the frequency axis from $f_{\min}=0$ to $f_{\max}=f_S$ depends on the number L of ADC basic modules.

General expression for evaluation of dynamic range of ADC is the following:

$$D = D_q + \Delta D_S - \Delta D_\tau, \tag{5}$$

where: D_q – dynamic range resulting from the quantization for an ideal ABC; ΔD_S – increase in dynamic range at the expense of superfluous discretization mode; ΔD_τ – losses in dynamic range at the expense of phase instability.

The last component of the expression (5) in consideration of (4) can be depicted as:

$$\Delta D_\tau = 20\lg\left(\frac{1}{m_l}\right) + 10\lg\left(\frac{4\pi^2(L-1)}{L}\right). \tag{6}$$

Taking into account that the component $10\lg\left(\frac{4\pi^2(L-1)}{L}\right)$ is a stable value, it can be considered that the noise characteristics of ADCP are affected mostly by aperture defect and the instability of fronts of discretization impulses. Thus, on the assumption of stable values of discretization frequencies and input signal frequencies, phase instability of a convertor must be lowered to expand dynamic range of ADCP.

The basis of the method of dynamic range improving of ADCP is the processing of output signal of ADC according to the expression (4). The sinusoidal signal can be used as a test signal The sinusoidal signal can be used as a test signal. On the one hand the frequency of the above-mentioned sinusoidal signal is limited by the requirements of Nyquist-Shannon theorem, that is, $0.5\cdot f_S$, but on the other hand it is limited by hardware complexity and the features of fast Fourier transform (FFT) algorithm, that is $0.05\cdot f_S$. If the number of discrete values on the output of ADC does not correspond the whole number of input signal cycles, then after applying FFT the effect of "spectrum spreading" is observed[11]. This effect is displayed with the appearance of high-frequency harmonics which distort the resulting spectrum and increase the noise level on the output of ADCP. To weaken this effect, window weighting is used. But the additional operations which have to be performed before FFT to implement the window weighting, cause the decrease of resulting operating speed of ADC[12-15].

Taking into account that a sinusoidal signal is a test signal, for the minimization of parasite components of the spectrum coherent discretization is applied, which requires the presence of whole number of cycles of input signal in discretization intervals. At the same time, there are no breaks on the edges of sinusoidal test signal. The mode of coherent discretization is provided with the following correspondence between the input signal frequency f_{in} and discretization frequency f_S :

$$\frac{f_{in}}{f_S} = \frac{K}{L}, \tag{7}$$

where: K – number cycles of input signal in process interval.
For the whole number of signal cycles the number K is prime and odd: $K = 1, 3, 5, 7$. After solving the algorithm FFT according to (4) the resulting complex spectrum is processed to define time shift τ_{al} for every L basic ADC. The received values of delays are the basis for correction of phase parameters of discretization impulses of ADC modules.

The structure chart of high-speed ADCP which shows the given method of correction of phase jitter is depicted in the Fig. 3. Output digital signal of ADC goes into digital processing unit (DPU) where the algorithm of FFT with coherent discretization and further evaluation of correction factors is realized. The information about the correction level of phase shifts between isolated discretization impulses goes out off DPU into forming unit of discretization impulses (FUDI). Time corrected discretization impulses go from output of FUDI to corresponding strobe-inputs of ADC modules.

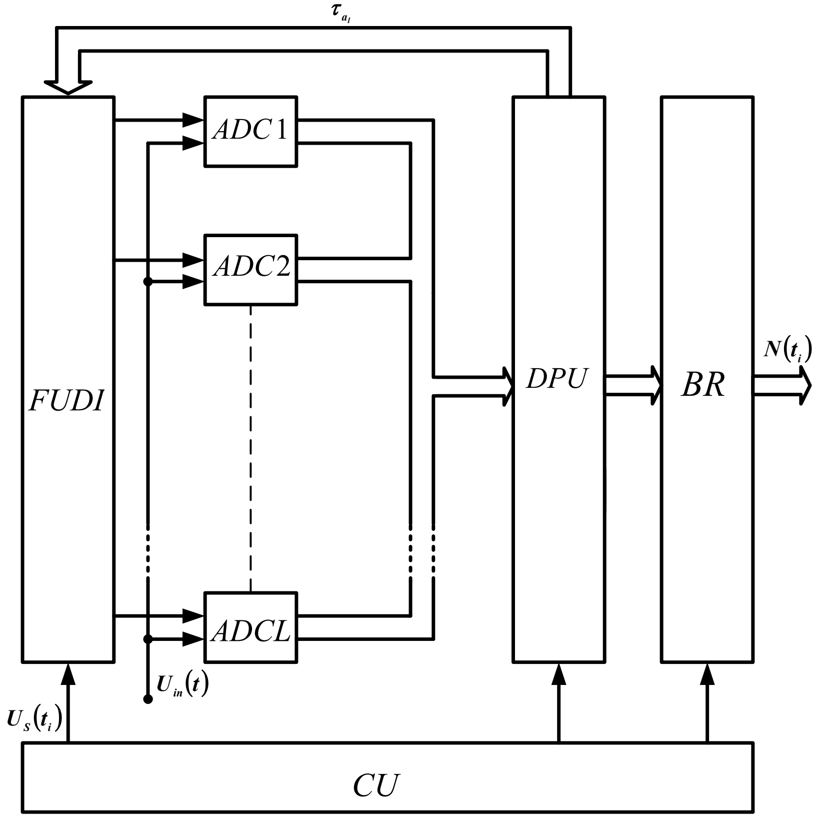

Figure 3. The structure chart of high-speed ADCP with the correction of phase jitter.

Due to the signal from the control unit (CU) final result of analog-to-digital conversion appears on output bus of buffer register (BR). The effectiveness of the developed method can be evaluated due to the advantages in the dynamic range during analog-to-digital conversion of the signals of intended frequency. There to the expression (5) must be depicted in a detailed form. It is known, that the dynamic range caused by the quantization for an ideal ADC of sinusoidal signal is defined in the following way[7]:

$$D_q = 6.02n + 1.8\,, \tag{8}$$

where: n – the number of bits of ADC.

It is easily observed that the dynamic range improves to 6 dB, that is 2 times, with the increase of ADC bit capacity. The discretization of PJ signals is implemented due to the requests of Kotel'nikov-Nyquist theorem. In case of the discretization with the frequency f_S that exceeds the maximum frequency in the input signal band more than twice, the mode of redundant discretization is observed. The advantage at the expense of the mode is defined as[9]:

$$\varDelta D_S = 10\lg\frac{f_S}{2f_{in}}\,. \tag{9}$$

The relation $\frac{f_S}{2f_{in}}$ is determined as an excess frequency ratio:

$$K_f = \frac{f_S}{2f_{in}}\,. \tag{10}$$

If $K_f = 4$ it is possible to improve the signal-to-noise ratio to 6 dB but in so doing it is necessary to apply ADCs which feature 4 times better operation speed in comparison with the classical way of discretization.

Substituting (8) and (9) into the relation (5) and taking into account the formula (6), the analytic expression for the evaluation of the dynamic range of ADC with the correction of phase instability of samples is derived:

$$D_T = 6.02n + 10\lg\frac{f_S}{2f_{in}} - 20\lg\frac{1}{m_l} - 10\lg\frac{4\pi^2(L-1)}{L} + 1.8. \tag{11}$$

The correction level $\Delta\tau_a$ evaluated by separating power of the algorithm of FFT which depends on the volume of the processed sample N and normalized pass band of data window β_ω. Therefore, secondary results processing of analog-to-digital conversion on the basis of FFT gives additional advantage to the dynamic range:

$$\varDelta D_{FFT} = 10\lg\frac{N}{2\beta_\omega}\,. \tag{12}$$

According to the expressions (11) and (12) it is possible to analyze the dynamic range of ADC which are constructed on the basis of the suggested method. The dependencies of the dynamic range of ADC on the amount of processed sample for variable values of the phase instability of basic 10-bit ADC are depicted in Fig. 4 and 5. Fig. 4. shows the graphs when ADC are constructed on the basis of the convertors modules which are characterized with 10-percentage deviation of phase shift, that is $m_l = 0.9$.

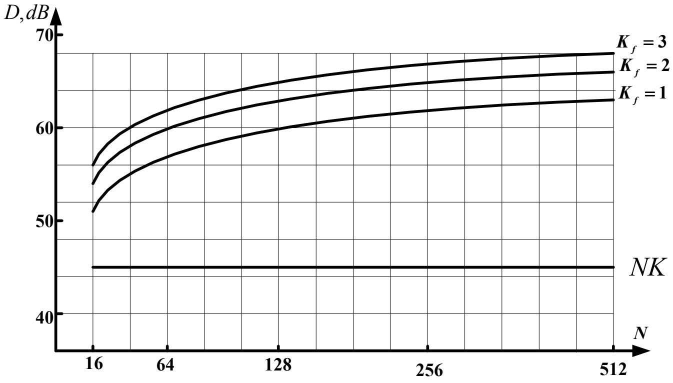

Figure 4. The dependence of the dynamic range on the volume of the processed sample of 10-bit ADCP for 10-percentage instability coefficient.

On such conditions the dynamic range with no correction equals 45 dB (lower straight line). Three upper curve lines are drawn for various values of coefficient of frequency redundancy. For the most upper curve $K_f = 3$ and for the other graphs correspondingly $K_f = 2$ and $K_f = 1$. Depending on the volume of the processed sample the dynamic range increases to the values 51÷67 dB that is 6÷22 dB better than for ADC with no correction.

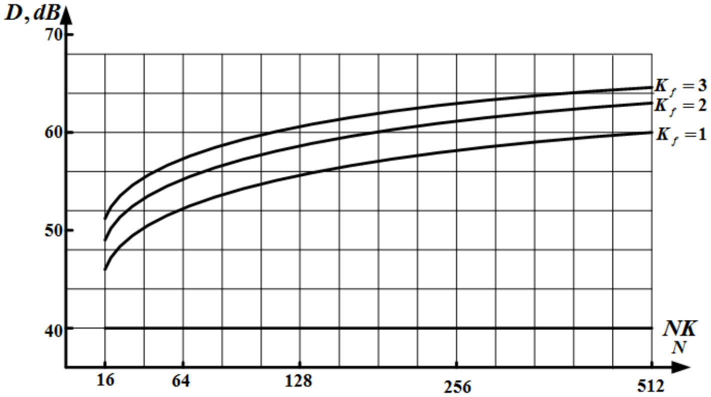

Figure 5. The dependence of the dynamic range on the volume of the processed sample of 10-bit ADCP for 50-percentage instability coefficient.

Similar results are derived at 50-percent deviation of the phase shift (Fig. 5.). At the same time for $m_l = 0.75$ the non-corrected dynamic range equals 43.5 dB and the corrected dynamic range increases to 49.5÷66.5 dB depending on the amount of the processed sample. Finally, for maximum phase instability $m_l = 0.5$ the non-corrected dynamic range equals 40 dB and the corrected dynamic range equals 46÷63 dB.

5. CONCLUSIONS

The analog-to-digital conversion path of PJ signals is the most important in the estimation process of FOTS jitter since the main dynamic parameters of ADCP have direct influence on the functioning effectiveness of PJ estimation means. The method of improving of dynamic range of ADCP of jitter analyzer is suggested which defines that dynamic parameters of ADC are greatly affected by marking-offs jitter of some convertors modules. The marking-offs jitter appears in consequence of aperture defect of ADC and phase jitter of clock fronts of discretization impulses. It is suggested to value phase instability of each of ADC modules according to the developed method of improvement of dynamic parameters of ADCP. It is done for the purpose of further correction by feedback circles of phase shift of discretization pulses. The analysis of dynamic range for the suggested method has shown that in comparison with the classical approach to analog-to-digital conversion the suggested method of phase shift correction of signal samples in ADCP gives the opportunity to expand the dynamic range up to 6÷22 dB depending on the instability coefficient and the processed sample of ADC.

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