УДК 621.396 DOI https://doi.org/10.32782/1995-0519.2023.2.22

# SYNTHESIS OF A DIGITAL FREQUENCY COUNTER ON PROGRAMMABLE LOGIC INTEGRATED CIRCUITS

**Andriy Semenov**
Doctor of Technical Sciences, Professor, Department of Information Radioelectronic Technologies and Systems
Vinnytsia National Technical University, 95 Khmelnytske Shosse, Vinnytsia, Ukraine, 21000, semenov.a.o@vntu.edu.ua
**ORCID: 0000-0001-9580-6602**

**Oleksandr Stalchenko**
Ph.D., Associate Professor, Department of Infocommunication Systems and Technologies
Vinnytsia National Technical University, 95 Khmelnytske Shosse, Vinnytsia, Ukraine, 21000, magicphenix@gmail.com
**ORCID: 0000-0003-4764-1502**

**Maksym Prytula**
Ph.D., Assistant Department of Information Radioelectronic Technologies and Systems
Vinnytsia National Technical University, 95 Khmelnytske Shosse, Vinnytsia, Ukraine, 21000, pritulamo@ukr.net
**ORCID: 0000-0003-1577-5215**

**Oleksandr Donskyi**
Postgraduate Student at Department of Information Radioelectronic Technologies and Systems
Vinnytsia National Technical University, 95 Khmelnytske Shosse, Vinnytsia, Ukraine, 21000, tiger119943@gmail.com
**ORCID: 0009-0007-7023-2076**

**Olha Voitsekhovska**
Ph.D., Assistant Department of System Analysis and Information Technologies
Vinnytsia National Technical University, 95 Khmelnytske Shosse, Vinnytsia, Ukraine, 21000, olgav1085@gmail.com
**ORCID: 0000-0001-8504-1204**

This work is dedicated to the synthesis of a digital frequency counter and the selection of its hardware implementation. The paper considers two frequency measurement methods: the discrete counting method and the filling method. In order to better understand the principles of these methods, structural diagrams of frequency counters based on them were developed. The authors examined the advantages and disadvantages of different hardware platforms such as rigid logic chips, microcontrollers, and programmable logic integrated circuits (PLIC) technology. It was found that rigid logic chips do not meet the requirements for small size and have limited capability for arithmetic operations. Although microcontrollers have small dimensions, they are characterized by low operating frequencies, which may be insufficient for certain applications. The use of PLIC technology proved to be the most optimal solution as it combines high operating frequency, small size, and affordable cost. In this work, the authors synthesized a high-precision frequency counter using PLIC technology. PLIC technology provides potential for the development of control and measurement equipment that can compete with standard devices. The achieved results indicate that the chosen hardware platform based on PLIC technology proved to be effective and allows for obtaining high-precision frequency measurement results in the frequency range up to 1 MHz. In the practical part of the work, a prototype frequency counter was developed based on the selected structural diagram. Added frequency synthesizer blocks and input selector enable verification of measurement accuracy and the use of various input signals for measurement. The development of the prototype involved the use of ALTERA microchips and the Quartus CAD system. The obtained results can be used in further research and development in the field of control and measurement technology. Based on the results, new devices for accurate frequency measurement can be developed for various fields such as telecommunications, medical diagnostics, scientific research, and many others.

The synthesized frequency counter based on PLIC technology represents an efficient device with accurate frequency measurements. Its dimensions and material costs are optimal, making it attractive for a wide range of applications. The experimental results confirm the high accuracy and efficiency of the proposed frequency counter.

**Key words:** frequency counter, PLIC, ALTERA, measurement.

**Introduction.** The development and improvement of control and information processing systems are largely determined by the widespread adoption of digital technology [1]. This is due to the well-known advantages of digital devices compared to analog ones, such as reliability, high stability of parameters, and high accuracy of information processing. Additionally, digital devices can incorporate adaptation algorithms, which are crucial for building highly efficient information processing systems [2].

The aim of this development is to synthesize a digital frequency counter for high-precision measurement of the frequency of periodic signals. These devices find wide application both in everyday life and in production. They can be standalone products or functional units of even more complex devices [3]. The accuracy, speed, and reliability of these devices largely depend on the underlying hardware platform on which the developed device is implemented. Therefore, it is important to utilize the latest hardware platforms. However, it is quite challenging to meet this requirement at present.

The modern development of computer technology allows for high-quality design of digital devices even in domestic conditions, before their physical implementation. Circuit design software packages such as Electronics Workbench, Microcap, and Quartus [4] greatly facilitate the work of circuit designers. They enable obtaining design results that are as close as possible to reality without physically building the device.

**Overview of methods of building frequency meters.** Frequency meters play a crucial role in radio engineering laboratories and are widely used for measuring the frequency of periodic signals. As a result, there are numerous methods available for frequency measurement [5]. The main methods include the resonance method, capacitor charge-discharge method, bridge method, discrete counting method, and fill method.

The resonance method is based on comparing the measured frequency with the resonant frequency of an oscillating circuit. It is applied for measuring frequencies ranging from 100 kHz to 100 GHz. The key component of a resonance frequency meter is the oscillating system. For frequencies up to 100 MHz, resonant circuits with lumped parameters are used, while for higher frequencies up to 1 GHz, circuits with distributed parameters in the form of coaxial or strip lines are employed. At even higher frequencies, volumetric resonators are used, and for frequencies above 30 GHz, open resonators are employed [6].

The capacitor charge-discharge method involves measuring the discharge current of a capacitor that is periodically recharged according to the measured frequency. The energy obtained during charging is equal to the energy consumed by the microammeter. Therefore, the amount of energy flowing through the microammeter per second represents the average value of the discharge current over the period. The readings of the microammeter are proportional to the measured frequency. Capacitive frequency meters are used for measuring frequencies ranging from 10 Hz to 500 kHz with a basic accuracy of 2%, at input voltage levels of 0.5 V to 200 V [7].

The bridge method is based on using frequency-dependent alternating current bridges powered by the measured frequency. It is used for measuring low frequencies within the range of 20 Hz to 20 kHz with a measurement error of 0.5–1%. An electronic millivoltmeter is employed as the balance indicator. The presence of harmonics complicates the balancing process due to the non-sinusoidal nature of the measured frequency, resulting in increased measurement errors [8].

The discrete counting method is based on counting the number of periods of the measured frequency within a known time interval. This method offers the highest measurement accuracy but requires the inclusion of as many periods of the input signal as possible within the measurement time interval. For example, if 1000 periods of the input signal can fit into the measurement time interval, the measurement error will be ±1 period, which is a good indicator. This method is used for measuring frequencies above 100 Hz, with the upper frequency limit determined by the speed of the employed components [9].

The fill method is similar to the discrete counting method, but instead, it counts the number of pulses with a known period within the duration of one period of the measured signal. This method is used when the frequency of the input signal is relatively low, such as 1 Hz. By filling a time interval of 1 second with pulses having a period of 1 ms, the measurement error will also be ±1 pulse.

All of the discussed methods enable frequency measurement in laboratory conditions. However, the first three methods have relatively high measurement errors. The resonance method depends on the quality factor of the resonant circuit, the capacitor charge-discharge method is affected by parameter variations of the capacitor and the quality of the microammeter's magneto-electric system, while the bridge method requires continuous balancing, the use of precision components, and is designed for measuring only sinusoidal signals.

The most accurate and stable methods are the fill method and the discrete counting method [10; 11].

However, each of them is not suitable for wide-range frequency measurement. Frequency meters that combine these two methods either have large dimensions or high cost. Therefore, the practical task arises to develop a digital frequency meter that combines these two methods and covers a wide frequency range.

**Development of a structural diagram of a digital frequency meter.** First, to address the problem of selecting an element base that would allow combining the methods of discrete counting and filling, it is necessary to create structural diagrams of frequency counters based on these principles.

Therefore, Figure 1 shows the structural diagram of a digital frequency counter that utilizes the method of discrete counting. The input signal is fed into the input of the up-counter, which is controlled by the reset signal from the frequency divider of the quartz generator. The output value of the counter is sent to the storage block where it is stored until the measurement display takes place. The integration time ($T_{int}$) is typically chosen to be around 1 second, which is sufficient for reading the information. ($T_{int}$) is the time during which we perform the counting of the number of pulses of the measured signal.

Figure 2. Structural diagram of a digital frequency counter based on the filling method.

In this case, the counter counts the number of filling pulses and is reset by the input signal. If we have a filling period duration of, let's say, 1 μs, then the counter output will represent the duration of the input signal period. Therefore, to display the frequency, we will use an arithmetic divider:

$$\nu = \frac{1}{T}, \qquad (1)$$

Where $\nu$ – represents frequency, and $t$ – represents period.

As a result of performing this operation, the frequency value will be displayed on the block indicators.

If we analyze both structural diagrams, we can see that they have the same blocks. The difference between them lies only in the fact that in Figure 2, the input frequency and the divider signals are swapped, and an arithmetic divider is used in the second structural diagram.

Based on this, we can choose the component base. Let's consider the advantages and disadvantages of building the device using rigid logic chips, microcontrollers, and programmable logic devices (PLIC).

Rigid logic chips cannot meet our requirement for achieving small dimensions because implementing the necessary circuits would require a large number of chips. Moreover, this would reduce the device's reliability. It is also challenging to perform arithmetic division using rigid logic chips, although they have lower cost and higher operating frequencies.

The possibility of reducing the size arises when using microcontrollers [6]. They allow for arithmetic division with sufficient accuracy, precise counting, and have small dimensions and weight. However, a drawback of widely available microcontrollers is the low working frequency of the quartz resonator. For example, microcontrollers from ATMEL have a maximum operating frequency of 16 MHz, which is insufficient for laboratory conditions. There are specialized microcontrollers with higher working frequencies, but their cost prohibits their widespread use.

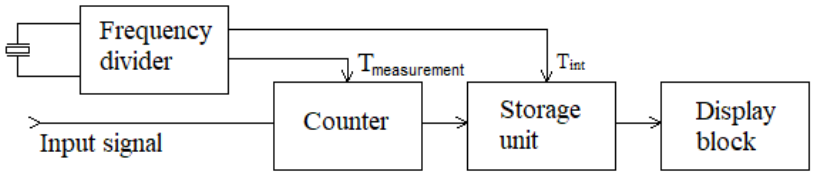


Fig. 1. Structural diagram of a digital frequency counter based on the principle of discrete counting

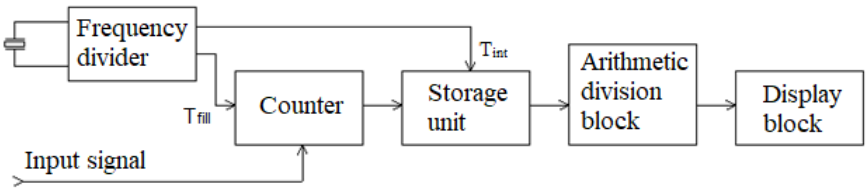


Fig. 2. Structural diagram of a digital frequency counter based on the principle of filling

The third option is the use of PLIC technology. Despite its limited popularity, this technology has relatively low cost. For example, non-specialized chips from ALTERA [6] can cost between $20 and $30. Their clock frequency can reach 250 MHz, and they can have up to 14,400 programmable elements, allowing for the creation of digital devices of considerable complexity. Furthermore, it is possible to design and simulate the device using the Quartus software package [7], which enables device creation not only based on the element database but also using the AHDL programming language and parameterized element libraries.

Based on the above, it can be noted that for the development of a digital frequency counter that works using discrete counting methods and filling, programmable logic chips are the best choice. For the practical implementation of the frequency counter prototype, we will select ALTERA chips and the UP2 laboratory board from the same manufacturer.

**Synthesis of digital frequency counter blocks in the Quartus program.** For the validation of our selection justifications, a digital frequency counter based on the structural diagram shown in Figure 1 was synthesized. It operates on the method of discrete counting. The synthesis of digital frequency counter blocks was carried out using the Quartus software [7]. Unlike the structure in Figure 1, the authors added two blocks – a frequency synthesizer and an input selector. The frequency synthesizer generates signals with different frequencies, which can be used to verify the measurement accuracy. The digital frequency counter selects the signal whose frequency will be measured using the input selector block. The synthesized electrical circuit of the frequency divider block in Quartus is shown in Figure 3.

The input signal is fed into an 8-bit counter with a radix of 251 to divide the input signal to a frequency of 100 kHz. This signal then goes into the next 10-bit counter with a radix of 1000. As a result, at the output corresponding to the most significant bit, we obtain pulses with a frequency of 100 Hz. However, we cannot yet use them because it is better to use a “clock pulse” for synchronization, which is a short-duration pulse whose rising edge we will control. To create this pulse, we will input our pulses into the sync input of a synchronous D flip-flop with dynamic control, and on the D input, we will provide pulses from a reference generator. As a result, at the output of the flip-flop, we will obtain a pulse with a duration of 39.7 ns during the rising edge of the pulse from the counter output, which gives us pulses with a frequency of 1 Hz.

We will feed the most significant bit of the second counter into a decade counter, and at its output, we will obtain the desired pulses, which we will similarly convert into “clock pulses”. To properly display them, we need to turn off one of the decimal points on the indicators, so we will generate a high and low level using an inverter and 2 logic gates, AND and XOR. If we look at the truth tables for these elements, we will

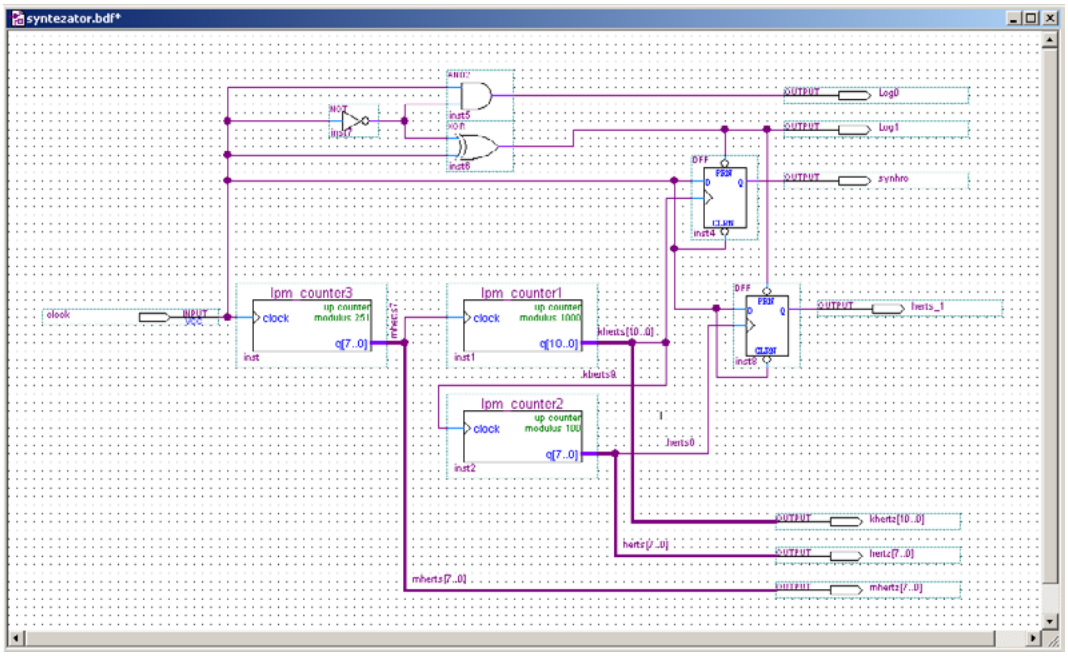


Fig. 3. Synthesized electrical circuit of the frequency divider block in Quartus

see that if different signals are present at the inputs of the AND gate, the output will be logic 0. Similarly, we obtain logic 1 at the output of the XOR gate.

The synthesized electrical circuit of the block in Quartus is presented in Figure 4.

The frequency counter block consists of four decade counters connected in parallel with respect to the sync inputs and in series with respect to the data inputs. The input signal we are measuring is applied to the input of the first counter. Then, at its output, tenths of the measured frequency will be generated at a frequency of 100 Hz. If we feed the most significant bit to the input of the second counter, we will obtain units at its output. Similarly, we generate tenths and hundredths of the input pulse count within 10 ms. Therefore, if we input 154.3 kHz, we will obtain the number 1543 at the counter output, and we only need to light up the corresponding decimal point on the display.

The storage block is organized based on a library of parameterized elements. Specifically, a 16-bit D flip-flop with dynamic control is created. It is synchronized with a 1 Hz signal and stores the frequency value obtained from the counter. All the counters used are also created based on parameterized elements. This also indicates the advantages of using FPGA technology, as it is challenging to obtain a counter with a radix of 251 using rigid logic chips.

The next block is the display block, whose electrical circuit in Quartus is shown in Figure 5. The display block consists essentially of a 16-bit D flip-flop and seven-segment code decoders. However, there is a problem in that we lack a two-digit display for displaying the frequency. Therefore, we will combine the microchips together. All the calculations will be performed by the FLEX10K due to its speed, and we will transmit the values of the two most significant bits through a jumper to the MAX7000S, which will simply perform the functions of two seven-segment code decoders. This will be the most optimal configuration. Of course, instead of using 8 outputs for transmission, we can use only 3 to transmit pulses to the two most significant counters and synchronization pulses, but this would increase the already significant error due to the asynchrony between the measurements of the higher and lower counters.

The frequency counter should perform accuracy verification of measurements. Therefore, an additional block has been introduced, which is a frequency synthesizer with frequencies of 0.8, 1.6, 25, 400, 200, and 100 kHz. The electrical circuit of the frequency synthesizer block is depicted in Figure 6.

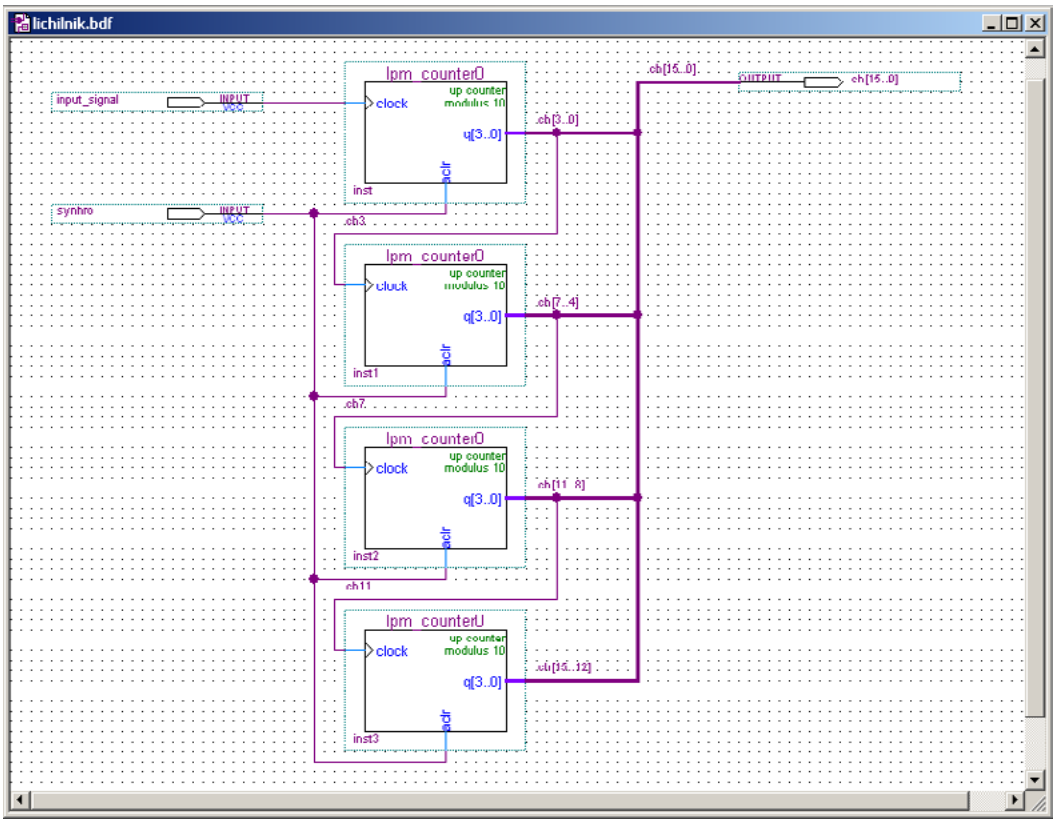


Fig. 4. Synthesized electrical circuit of the counter block in Quartus

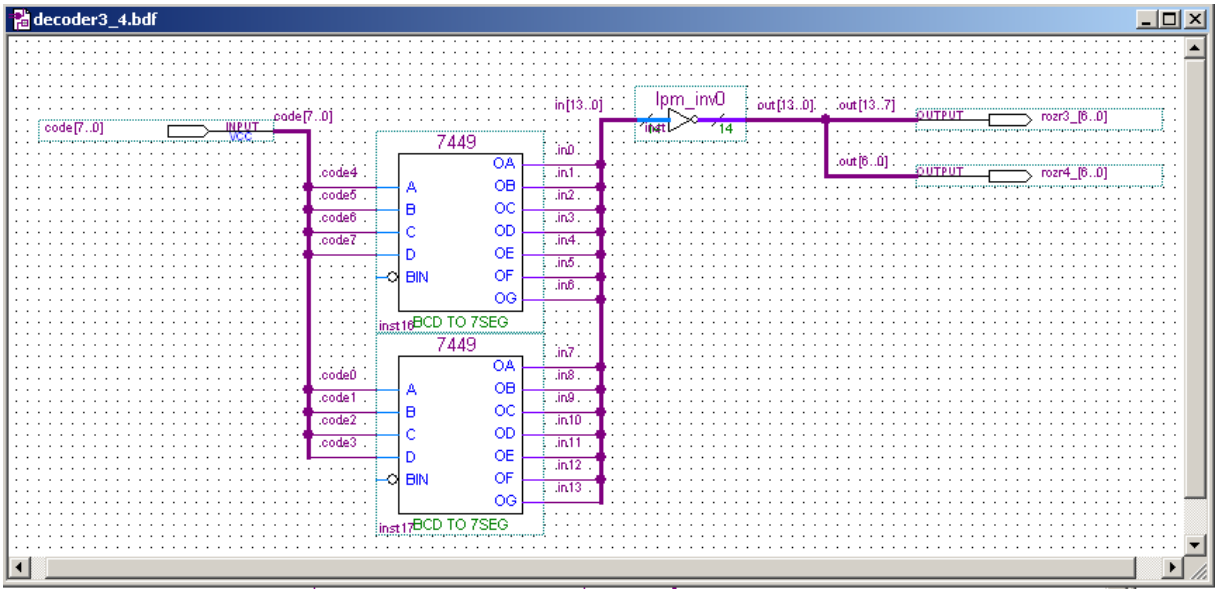


Fig. 5. Synthesized electrical circuit of the frequency value indication block in Quartus

It essentially functions as the same frequency divider, but it outputs a single signal that is taken from the outputs of the counters. The selection of the desired signal is accomplished using switches located on the board. The seventh switch feeds the input signal from an external source to the output of the synthesizer.

Results of the digital frequency counter research. The Quartus package includes a utility for device simulation, where input signals and simulation time can be defined. Let's choose a simulation time of 30 ms. This will be sufficient for the circuit to settle and for all processes to be observed. To investigate, we will display the main signals: the input signal from the reference generator, the states of the selection switches for reference signals, the sync pulse, the "needle" pulse, the output signal from the synthesizer, and the output digits. Specifically, the two least significant digits will be displayed in seven-segment code, while the two most significant digits will be displayed in a four-digit code.

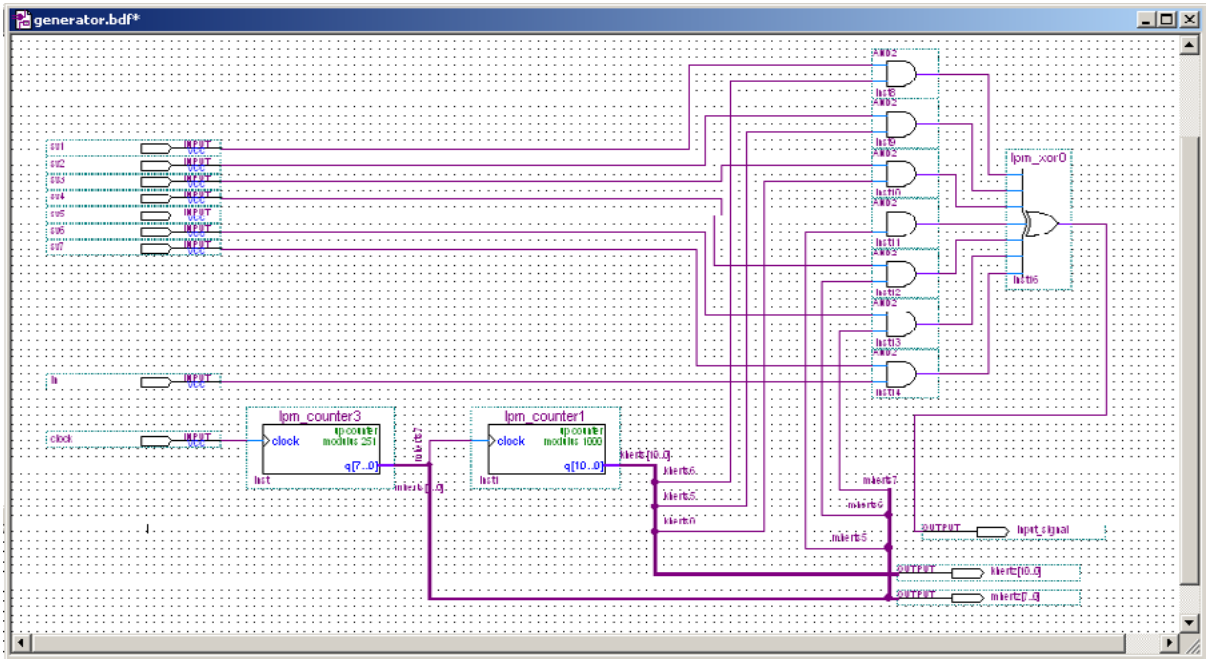


Fig. 6. Synthesized electrical circuit of the frequency synthesizer block in Quartus

Fig. 7 shows the process of forming the “needle” pulse from rectangular pulses with a 50% duty cycle. As a result, pulses with a period of 10 ms and a duration of 19 ns are generated. Considering that all the digital elements we use operate from the sync pulse’s rising edge, this will be entirely sufficient for our purposes.

As already described, the counter consists of 4 decade counters that directly count the input pulses and reset upon the arrival of the sync pulse rising edge. Figure 8 shows the waveforms of the input and output signals at a frequency taken from the synthesizer, which is 25 kHz.

As can be seen from the figure, after the first sync pulse, the counters are reset and begin counting until the next sync pulse occurs. At the same time, the D flip-flop “memorizes” the values of the signals at the outputs of the counters and sets them as inputs to the seven-segment decoders.

After examining the operation of the main components, let’s consider the operation of the entire device. The voltage waveforms are shown in Figure 9.

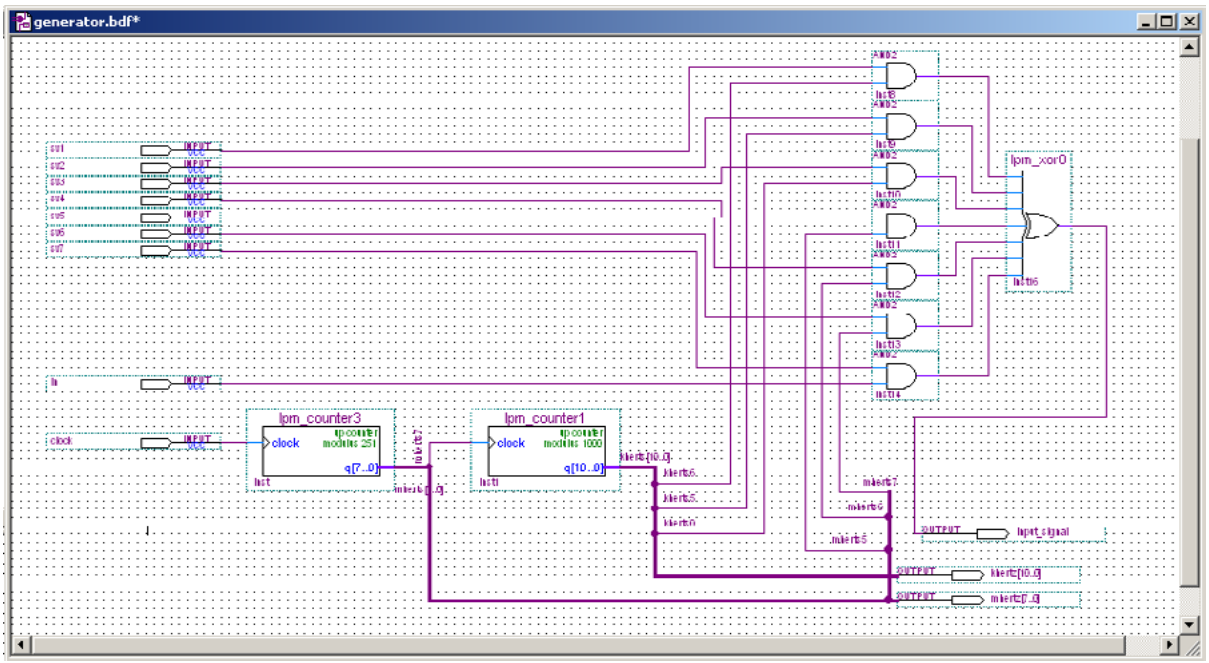


Fig. 7. Timing diagram of the sync pulse formation


Fig. 8. Simulation Results of the Counter Operation

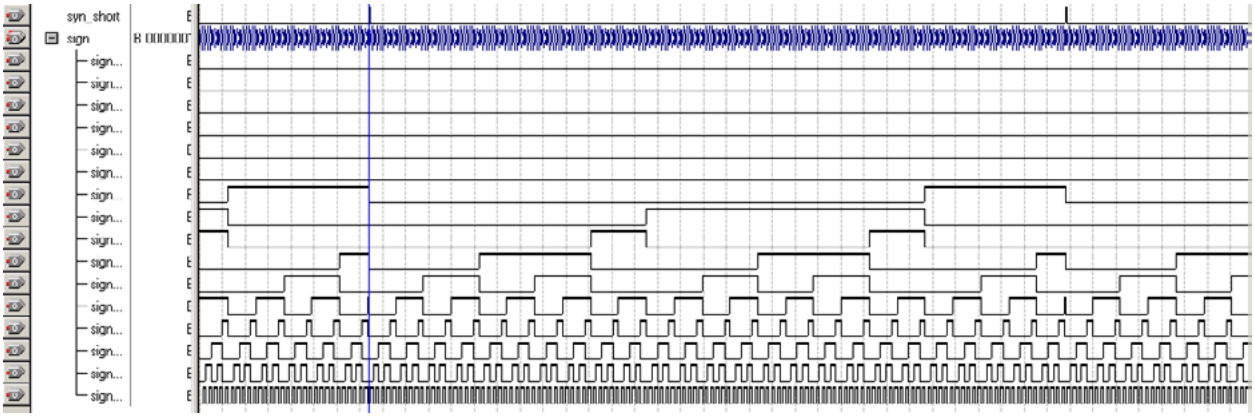


Fig. 9. Results of simulating the operation of the digital frequency counter

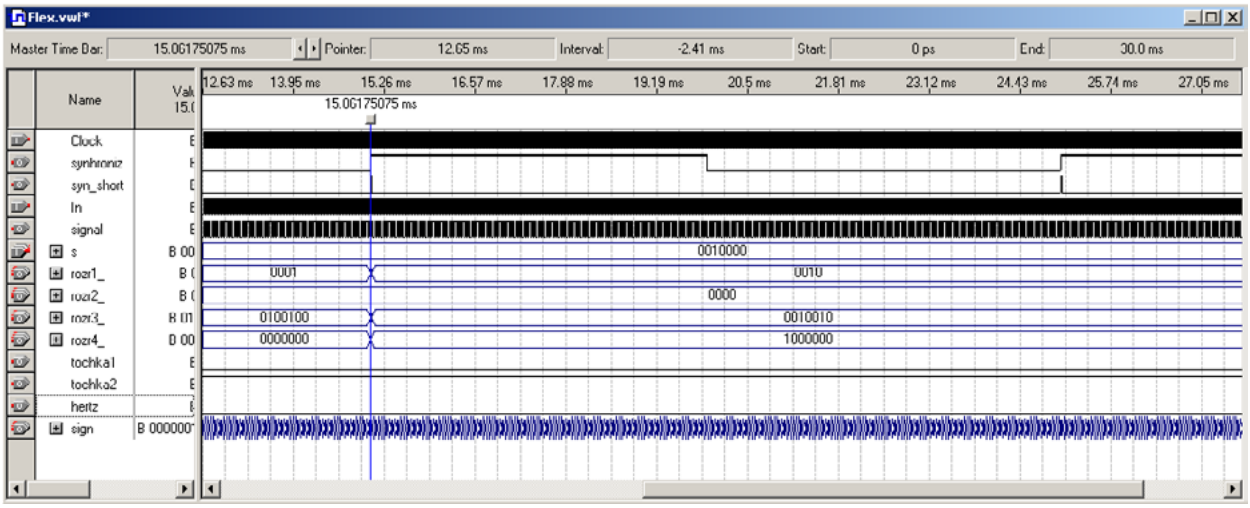


Fig. 10. Circuit diagram connecting the counters and binary-to-decimal decoders together

tco

| | Slack | Required tco | Actual tco | From | To | From Clock |
|---|---|---|---|---|---|---|
| 1 | N/A | None | 30.002 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[2] | Fx |
| 2 | N/A | None | 30.001 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[6] | Fx |
| 3 | N/A | None | 29.999 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[1] | Fx |
| 4 | N/A | None | 29.978 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[4] | Fx |
| 5 | N/A | None | 29.912 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[2] | Fx |
| 6 | N/A | None | 29.911 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[6] | Fx |
| 7 | N/A | None | 29.909 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[1] | Fx |
| 8 | N/A | None | 29.866 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | FF | Fx |
| 9 | N/A | None | 29.864 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[4] | Fx |
| 10 | N/A | None | 29.818 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[3] | HL5[2] | Fx |
| 11 | N/A | None | 29.817 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[3] | HL5[6] | Fx |
| 12 | N/A | None | 29.815 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[3] | HL5[1] | Fx |
| 13 | N/A | None | 29.814 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[2] | 1Hz |
| 14 | N/A | None | 29.813 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[6] | 1Hz |
| 15 | N/A | None | 29.811 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[1] | 1Hz |
| 16 | N/A | None | 29.790 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[4] | 1Hz |
| 17 | N/A | None | 29.773 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[3] | FF | Fx |
| 18 | N/A | None | 29.724 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[2] | 1Hz |
| 19 | N/A | None | 29.723 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[6] | 1Hz |
| 20 | N/A | None | 29.721 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[1] | 1Hz |
| 21 | N/A | None | 29.717 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[0] | HL5[2] | Fx |
| 22 | N/A | None | 29.715 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[0] | HL5[6] | Fx |
| 23 | N/A | None | 29.714 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[0] | HL5[1] | Fx |
| 24 | N/A | None | 29.705 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[3] | Fx |
| 25 | N/A | None | 29.686 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[5] | Fx |
| 26 | N/A | None | 29.683 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[0] | HL5[4] | Fx |
| 27 | N/A | None | 29.678 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | FF | 1Hz |
| 28 | N/A | None | 29.676 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[2] | HL5[4] | 1Hz |
| 29 | N/A | None | 29.630 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[3] | HL5[2] | 1Hz |
| 30 | N/A | None | 29.629 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[3] | HL5[6] | 1Hz |
| 31 | N/A | None | 29.627 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[3] | HL5[1] | 1Hz |
| 32 | N/A | None | 29.615 ns | lpm_counter1:inst16\|lpm_counter:lpm_counter_component\|cntr_nsh:auto_generated\|safe_q[1] | HL5[3] | Fx |

Fig. 11. Analysis of the delay time of individual components of the digital frequency counter on the PLIC

From the oscillograms, it can be seen that the output signals remain static for a duration of 10 ms. They do not change unless the input signal changes.

To determine the performance and other parameters of the digital part of the frequency counter implemented on the FPGA, we will perform analysis using the Quartus II software environment.

As seen in Figure 10, the main functional component that requires calculation is the binary-to-decimal decoders, as they provide the "commands" for the displays. Additionally, to increase the bit depth of the frequency counter, it is necessary to reset the counter to 0 when a certain number is reached and propagate the pulse to the higher-order counter. This number is $10_{10} = 1010_2$. To perform the reset, logical multiplication of the q1 and q3 outputs of the counter is applied, and the result is fed to the carry-in (C) input of the higher-order counter, simultaneously with the scl input of the main counter. The circuit diagram of this connection method is shown in Figure 10.

During compilation and simulation, the following data was obtained, as shown in Figures 11–13.

As seen from the obtained results, the frequency counter implemented on the PLIC can operate at the maximum frequency of around 33–45 MHz without loss of accuracy.

During the device modeling, the maximum signal propagation delay from input to output was measured at 38.500 ns, which is acceptable for measurements.

The frequency measurements of the synthesizer are shown in Table 1.

From Table 1, it can be observed that the developed frequency counter has decent parameters, as indicated by the small measurement error. However, there is an existing error, especially at the boundaries of the frequency range, which can be attributed to the high frequency of the synchronizing signal and the simplicity of the design.

Timing Analyzer Summary

| | Type | Slack | Required Time | Actual Time | From | To | From Clock | To Clock | Failed Paths |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Worst-case tco | N/A | None | 30.002 ns | lpm_counter1:inst16\|lpm_count... | HL5[2] | Fx | -- | 0 |
| 2 | Clock Setup: 'Fx' | N/A | None | 45.19 MHz ( period = 22.130 ns ) | lpm_counter1:inst16\|lpm_count... | lpm_counter1:inst\|lpm_counter:lp... | Fx | Fx | 0 |
| 3 | Clock Setup: '1Hz' | N/A | None | 45.19 MHz ( period = 22.130 ns ) | lpm_counter1:inst16\|lpm_count... | lpm_counter1:inst\|lpm_counter:lp... | 1Hz | 1Hz | 0 |
| 4 | Total number of failed paths | | | | | | | | 0 |

Fig. 12. Overall timing analysis of the digital frequency counter on the PLIC

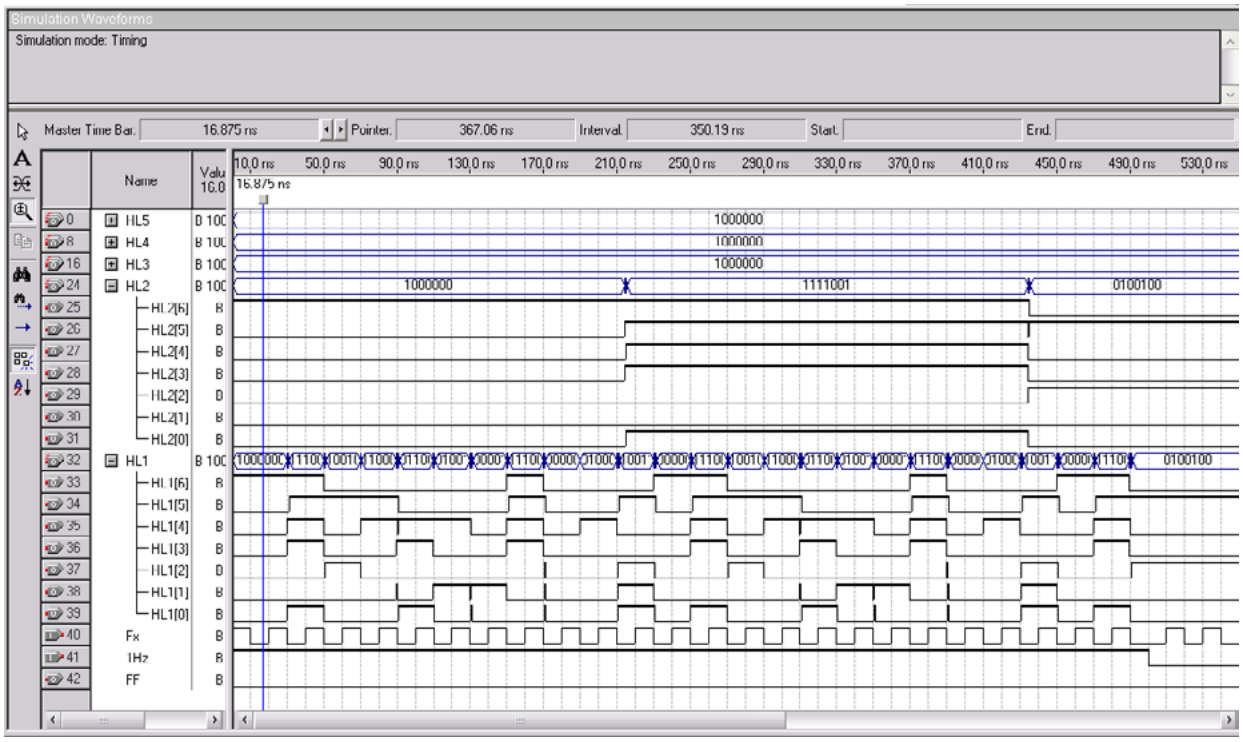


Fig. 13. Timing diagrams of the operation of the digital portion of the frequency counter on the PLIC

Table 1

**Frequency Measurement Error Evaluation Results**

| Input Signal Period | Input Signal Frequency, Hz | Indicator Value during Simulation | Indicator Value during Device Operation | Absolute Error, Hz | Relative Error, % |
|---|---|---|---|---|---|
| 1,275483439 мс | 784 | 0,8 | 0,8 | 16 | 2 |
| 637740825 мкс | 1568 | 1,6 | 1,6 | 32 | 2 |
| 39,858839 мкс | 25088 | 25,0 | 25,0 | 88 | 0,3 |
| 2,50818 мкс | 399,869 | 400,0 | 400,0 | 131 | 0,03 |
| 5,001257 мкс | 199,949 | 200,0 | 200,0 | 51 | 0,02 |
| 10,061358 мкс | 99,390 | 99 | 99,0 | 390 | 0,3 |

**Conclusions.** The authors conducted an analysis of various frequency counter construction methods to determine the most practical and accurate approach. They focused on analyzing different design solutions and identifying the optimal approach in terms of size and material costs for implementation. A functional frequency counter circuit was synthesized using ALTERA's PLIC technology, developed with the Quartus software. The synthesized circuit proved to be a successful solution for creating an efficient digital frequency counter.

An analysis of measurement errors was performed, revealing that the developed digital frequency counter demonstrates high accuracy in frequency measurement up to 1 MHz. The developed frequency counter is capable of competing with standard devices, considering its accuracy and potential for developing measurement and control equipment.

The PLIC-based frequency counter developed represents an effective device with precise frequency measurements. Its optimal size and material costs make it attractive for wide-ranging applications in various fields, including telecommunications, medical diagnostics, scientific research, and others.

Considering the optimal size and material costs of the developed frequency counter, it can be recommended for broad application in different industrial sectors and research areas.

The results of this work pave the way for further development and improvement of frequency counters using advanced technologies and measurement methods. The experimental results obtained by the authors confirm the high accuracy and efficiency of the proposed frequency counter.

This study contributes significantly to the body of knowledge regarding the construction of frequency counters and the selection of component bases for their implementation. The obtained results indicate the prospects of using PLIC technology for creating accurate and efficient frequency measurement devices.

## REFERENCES

1. Roger Tokheim & Patric Hoppe. (2022). *Digital Electronics: Principles and Applications*. McGraw-Hill Education. 644 p.

2. Anil K. Maini. (2007). *Digital Electronics: Principles, Devices and Applications*. John Wiley & Sons Ltd. 741 p.

3. Saleh Alsuhaibani, Yasin Khan, Abderrahmane Beroual & N.H. Malik (2016). A Review of Frequency Response Analysis Methods for Power Transformer Diagnostics. *Energies*, 9 (12): 879, pp. 1–17. DOI: 10.3390/en9110879.

4. Yang Liu, Jigou Liu &Ralph Kennel (2021). Frequency Measurement Method of Signals with Low Signal-to-Noise-Ratio Using Cross-Correlation. *Machines*, 9(123), pp. 1–17. DOI: 10.3390/machines9060123.

5. Yang Liu, Jigou Liu &Ralph Kennel (2021). Frequency Measurement Method of Signals with Low Signal-to-Noise-Ratio Using Cross-Correlation. *Machines*, 9(123), pp. 1–17. DOI: 10.3390/machines9060123.

6. Vakman D. (2000). New high precision frequency measurement. *Measurement Science and Technology*. № 11 (1493), pp. 1–23. DOI 10.1088/0957-0233/11/10/310.

7. Zhan, L., Liu, Y. & Culliss, J. (2015). Dynamic single-phase synchronized phase and frequency estimation at the distribution level, *IEEE Trans. Smart Grid*, 6(4), pp. 2013-2022. DOI: 10.1109/TSG.2015.2400973.

8. Marim Alan Phillimon, Salam Devayani Devi & Loitongbam Surajkumar Singh. (2019). A Review of Different Methods of Phase Measurement and its Suitable Applications. *In 2019 IEEE 5th International Conference for Convergence in Technology (I2CT)*, pp. 544–551. DOI: 10.1109/I2CT45611.2019.9033946.

9. K. Zhang, Y. Zhou, Z. Zou, W. Ding, and Z. Liu. Review on Frequency Measurement Techniques for Power Systems. *Sensors*, vol. 20, no. 19, 5432, September 2020. DOI: 10.3390/s20195432.

10. Wang, H., Ruan, Y., Yu, Y., Guo, Q., Xi, J., Tong, J. (2020). A new algorithm for displacement measurement using self-mixing interferometry with modulated injection current. *IEEE Access*, 8, pp. 123253–123261. DOI: 10.1109/ACCESS.2020.3007516.

11. Zeyad Assi OBAID, Liana M. CIPCIGAN, Lahieb ABRAHIM & Mazin T. MUHSSIN. (2019). Frequency control of future power systems: reviewing and evaluating challenges and new control methods. *Journal of Modern Power Systems and Clean Energy*. Vol. 7, pp. 9–25. DOI: 10.1007/s40565-018-0441-1.

# СИНТЕЗ ЦИФРОВОГО ЧАСТОТОМІРА НА ПРОГРАМОВАНИХ ЛОГІЧНИХ ІНТЕГРАЛЬНИХ СХЕМАХ

**Андрій Семенов**
доктор технічних наук, професор кафедри інформаційних радіоелектронних технологій і систем
Вінницький національний технічний університет, Хмельницьке шосе, 95, Вінниця, Україна, 21000, semenov.a.o@vntu.edu.ua
**ORCID: 0000-0001-9580-6602**

**Олександр Стальченко**
кандидат технічних наук, доцент кафедри інфокомунікаційних систем і технологій
Вінницький національний технічний університет, Хмельницьке шосе, 95, Вінниця, Україна, 21000, magicphenix@gmail.com
**ORCID: 0000-0003-4764-1502**

**Максим Притула**
кандидат технічних наук, асистент кафедри інформаційних радіоелектронних технологій і систем
Вінницький національний технічний університет, Хмельницьке шосе, 95, Вінниця, Україна, 21000, pritulamo@ukr.net
**ORCID:** 0000-0003-1577-5215

**Олександр Донський**
аспірант кафедри інформаційних радіоелектронних технологій і систем
Вінницький національний технічний університет, Хмельницьке шосе, 95, Вінниця, Україна, 21000, tiger119943@gmail.com
**ORCID: 0009-0007-7023-2076**

**Ольга Войцеховська**
кандидат технічних наук, асистент кафедри системного аналізу та інформаційних технологій
Вінницький національний технічний університет, Хмельницьке шосе, 95, Вінниця, Україна, 21000, olgav1085@gmail.com
**ORCID: 0000-0001-8504-1204**

Дана робота присвячена синтезу цифрового частотоміра та вибору елементної бази для його реалізації. У роботі розглянуто два методи вимірювання частоти – метод дискретного підрахунку та метод заповнення. Для кращого розуміння принципів роботи цих методів були складені структурні схеми частотомірів, що базуються на них. Автори розглянули переваги та недоліки різних елементних баз, таких як мікросхеми жорсткої логіки, мікроконтролери та технологія програмованих логічних інтегральних схем (ПЛІС). Виявлено, що мікросхеми жорсткої логіки не задовольняють вимоги до малих габаритів та мають обмежену можливість виконання арифметичних операцій. Мікроконтролери, хоча й мають малі габарити, відзначаються низькою робочою частотою, що може бути недостатньою для деяких застосувань. Застосування ПЛІС-технології виявилося найоптимальнішим варіантом, оскільки вона поєднує високу робочу частоту, невеликі габарити та доступну ціну. У роботі автори синтезували високоточний частотомір з використанням ПЛІС-технології. ПЛІС-технологія надає потенціал для розробки контрольно-вимірювальної апаратури, яка може конкурувати зі стандартними пристроями. Досягнуті результати вказують на те, що обрана елементна база на основі ПЛІС-технології виявилася ефективною і дозволяє отримати високоточні результати вимірювання частоти в діапазоні частот до 1 МГц. У практичній частині роботи було розроблено прототип частотоміра на основі обраної структурної схеми. Додані блоки синтезатора частот та вхідного селектора дозволяють перевірити правильність вимірювання та використовувати різні вхідні сигнали для вимірювання. Для розробки прототипу були використані мікросхеми фірми ALTERA та САПР Quartus. Дані результати можуть бути використані в подальших дослідженнях та розробках у сфері контрольно-вимірювальної техніки. На основі отриманих результатів можна розробляти нові пристрої для точного вимірювання частоти в різних галузях, таких як телекомунікації, медична діагностика, наукові дослідження та багато інших. Синтезований частотомір на основі ПЛІС технології становить ефективний пристрій з точним вимірюванням частоти. Його габарити та матеріальні затрати є оптимальними, що робить його привабливим для широкого застосування. Отримані експериментальні результати підтверджують високу точність та ефективність запропонованого частотоміра.

**Ключові слова:** частотомір, ПЛІС, ALTERA, вимірювання.

*Стаття надійшла 07.04.2023*