4. CONCLUSIONS

The author holds a course about Advanced Data Structures and Algorithms to 2-nd year students of the Technical College. The students have an 1 year experience in Pascal and they can understand more complex programming concepts, like dynamic data structures, programming techniques and algorithmic strategies.

However, they feel the tools to design, run, check and maintain a program are not adequate to modern times and the efficiency of coding is not very high. Moreover, it is supposed that the future graduates of Technical Colleges will not work as system engineers or high-skilled programmers, but as professionals whose tasks are well defined. They should be able to assembly together ready pieces of program, to assist in developing software projects. That's why to teach them data structures not by using Pascal, but rather using class libraries in C++ is a challenge that they are able to undertake.

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THE ANALYSIS OF RECOGNITION SEQUENCES' STRUCTURE AND APPLICATION POINTS FOR DIGITAL COMPONENTS IDENTIFICATION

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Abstract. *As concerning the identification of a component in a structure of printed circuit boards (PCB) of electronic device in this paper the solution of problems' set connected with revealing of components' location and recognition of its type or function performed by it are meant. As a component, in this case, can be any functionally or structurally extracted part of PCB from a separate chip, up to some fragment of device.*

The approach to the identification stimulus and their application points' choice in the digital components (DC) of the type "black box" identification using in-circuit tester are discussed in the report.

Introduction

The problem of electronic components' in-circuit identification in printed circuit board (PCB) of unknown structure [1,3] appears when solving such tasks as:

- restoring PCB functional diagram in case of technical documentation lack or with existing changes of diagram which is not reflected in this documentation [1];
- automated test program generation is realized in the in-circuit tester self learning mode (in this case studying PCB may be defective) [3];

• realizing adaptive inference mechanism to extended in-circuit tester fault directories [4].

• device verification in cases when necessary to exclude possibility of a discrepancy between an object and the present documentation.

A result of identification is a graphical image of printed circuit board which represents PCB components, lists of their characteristics and links between them, and a result of verification is a protocol printing, including messages about a direction of differences between an object functional diagram and the present documentation..

One of the main problems, solved during identification, is choosing of identificating stimulus application points in condition of apriori information absence about belonging a component D_j specified pins to subset of one's inputs X_j or outputs Y_j.

Formal description of the object of identification

The suggesting approach to the problem of DCs D_j identification is based on the following representation of their structural and functional properties [1,3]:

1) structural properties vector $Z(D_j)$ (SPV) the length of which coincides with number of component pins, and its coordinates' values are defined as following:

$$z_{i,j} = \begin{cases} 1, & \text{if } v_{i,j} \in X_j; \\ 0, & \text{if } v_{i,j} \in Y_j. \end{cases} \qquad (1)$$

where X_j – set of component inputs, Y_j -- set of component outputs, and $V_j = X_j \cup Y_j$ -- set of component pins. In common case are $Xj \cap Y_j \neq \varnothing$;

2) DC functional-algebraic model (FAM):

$$F_j = \left\{ f_{i,j} \;\middle|\; i = \overline{1, |Y_j|} \right\}, \qquad (2)$$

where $f_{i,j}$ -- elementary function which reflects dependence of the D_j output $y_{i,j} \in Y_j$ state on states of D_j inputs certain subset $X_{i,j} \subset X_j$ in algebraic form [1].

For example, the state of component SN72LS74 output Q_1 will be described as following:

$$Q_1 = (1 - S_1) + S_1 \times R_1 \times \left[Q_1^{\alpha} + C' \times \left(D_1 - Q_1^{\alpha} \right) \right],$$

where Q^{α} -- the output Q state at the previous test step; C' - the clock input.

3) DC structural-functional algebraic model (SFAM) which reflects complex of DC's structural and functional properties:

$$F(D_j) = \sum_{i=1}^{|V_j|} 2^{i-1} \cdot f_{i,j}, \qquad (3)$$

where

$$f_{i,j}^{*} = \begin{cases} v_i, & \text{if } v_{i,j} \in X_j; \\ f_{i,j}, & \text{if } v_{i,j} \in Y_j. \end{cases} \qquad (4)$$

4) component state code (CSC):

$$n_j^t = \sum_{i=1}^{|V_j|} 2^{i-1} \cdot b_{i,j}^t \qquad (5)$$

where $b_{i,j}^t$ -- the values of signals' levels which are present at the moment of time t at the D_j outputs.

5) DC state's space obtained from SFAM (3) by means of substitution of all the possible input signals' combinations:

$$N_j = \left\{ n_j^k,\ k = \overline{1,m} \right\},$$

where $m \le 2^{|X_j|}$ for DC without memory and $m \le 2^{|V_j|}$ for DC with memory.

6) the state search which is represented by matrix $M = \left\| m_{i,j} \right\|$, the rows of which define the allowable state codes of all components which descriptions are saved in the references' library, and the columns - the types of this components:

$$m_{i,j} = \begin{cases} 1 & \text{if } n_j^i \in N_j, \\ 0 & \text{if } n_j^i \notin N_j \end{cases} \qquad (6)$$

Single-digit distinguishing stimulus

We will name the vector B_S^α of dimension $|V_{S,j}|$, coordinates of which map logical signals values, applicated urged on the subset $V_{S,j}$ of DC D_j the pins at the some moment of time *t*, as a testing stimul (TS) φ_S^α .

The component D_j state transition from n_j^k to n_j^m [1], implemented during TS φ_S^α application, we will designate in the following form:

$$n_j^k \xrightarrow{f(\varphi_S^\alpha)} n_j^m . \qquad (7)$$

The set Π_j of testing stimulus, ensuring transitions (7), which fulfill the condition:

$$\left\{ n_j^k, n_j^m \right\} \in N_j, \qquad (8)$$

we will name as a set of identificating stimulus (IS), and IS sequences will be identificating sequences. Note, that because of CSC (5) takes into account the states of all pins of

identificated component (as outputs so inputs), then all TS, fulfilling the condition (8), including ones which do not cause change of any pin state, refer to IS.

The absence of the apriori information about the values of SPV $Z(D_j)$ coordinates and the set N_j of the component D_j allowed states during identification causes real opportunity of TS application not to the inputs only, but to the outputs of DC too, as a result one can be urge switched to the state $n_j^m \notin N_j$. At the same time, for assured fulfillment of the condition:

$$\varphi_S^\alpha \in \Pi_j, \qquad (9)$$

it is necessary to ensure TS application only to the inputs of the identificated component D_j. In connection with this, during choosing the basic IS it is necessary to take into account the following:

1. If an information about the set N_j of allowed component states is absent, then fulfillment of the condition:

$$\left(\exists \hat{v}_{i,j} \in V_j \right) \Big| \left[(\hat{v}_{i,j} \notin V_{S,j}) \wedge (b_{i,j}^t \ne b_{i,j}^{t-1}) \right], \qquad (10)$$

ensures that the situation

$$V_{S,j} \cap X_j \ne \varnothing \qquad (11)$$

takes place during IS φ_S^α application to the subset $V_{S,j}$ of component D_j inputs at the moment of time *t*.

2. Actions (as testing so identificating) which fulfill the condition (11), we will name as distinguishing stimulus.

The fulfillment of the condition (8) can be assured only if the condition (11) and

$$|V_{S,j}| = 1 \qquad (12)$$

are fulfilled simultaneously.

The identificating stimul φ_S^α , which fulfills the conditions (10) and (12), we will name the single-digit distinguishing stimul (SDS).

So, TS φ_S^α , which fulfills the condition (12), is the most informational from the point of a component type identification, because it allows to make the following conclusions at a registration of the condition (10) fulfillment during the identification:

$$\varphi_S^\alpha \in \Pi_j; \qquad n_j^m \in N_j; \qquad V_{S,j} \subset X_j; \qquad \hat{v}_{i,j} \in Y_j$$

Note, that SDS is elementary IS executed in two clock times t and $t+1$, during the first of which the pin $v_{k,j} \in X_j$ is switched in some urge state, and during second it returns to the initial state, i.e. the following relationship takes place:

$$b_{k,j}^t \neq b_{k,j}^{t+1} = b_{k,j}^{t-1}.$$

Reference components representation by n-graphs.

Let's represent DC D_j by a graph $G_j = \langle (Q_j, N_j), (E_j, \Pi_j) \rangle$. The set Q_j of the graph vertices maps the set of the allowed component states and each vertex is marked by the corresponding code $n_j^k \in N_j$ and the set E_j of the edges maps the sets of the component allowed transitions from one state to another. Thus, each edge marked by code causing the transition (8) IS φ_S^α Π which includes the list of IS application points (subset V_S, of set component pins) and the logical levels of stimulus applicated to these points.

The graph G_j can be easily formed from SFAM (3) of the corresponding component D_j and used for obtaining of the optimal identificating sequences.

Let's consider n-graph G_j^n family, the edges of which map the corresponding sets of IS $\{\varphi_S^\alpha\}$, fulfilling the condition $|V_S|$=n. Let's define the graph G_j^* as 1-graph with the set of the edges which maps the set of SDS. Each edge is described by a vector in the form $< n_j^k, v_{k,j} >$, where $v_{k,j} \in V_{S,j}$ is a number of the pin on which SDS is applied.

Let's change in the matrix (6) values of the elements $m_{i,j}$=1 by sets $V(q_{i,j})$ of pins numbers describing the edges, originating from the corresponding vertices $q_{i,j}$ of the graph G_j^*. Then let's form the matrix M^* by introducing the additional columns $m_1^*, \ldots, m_{|V_j|}^*$, corresponding to pins' numbers of the reference components, into the matrix M. The values of the additional elements $m_{i,p}^*$, $p = 1, |V_j|$ will be determined as the following:

$$m_{i,p}^* = \sum_{j=1}^{J} \mu_{i,j},$$

where J — is a number of the components' descriptions in the reference library,

$$\mu_{i,j} = \begin{cases} 1, & \text{if } v_{p,j} \in V(q_{i,j}) \\ 0, & \text{if } v_{p,j} \notin V(q_{i,j}) \end{cases}.$$

Representation of a search space by the matrix M^* facilitates the solution of the problem of SDS application points' choice during the component D_j identification in the conditions of apriori information about one's SPV absence.

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KNOWLEDGE-BASED ALGORITHM OF HYBRID ELECTRONIC DEVICES IDENTIFICATION

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Abstract. *The algorithm of in-circuit components' and electric connections' identification into printed circuit boards (PCB) of the hybrid electronic devices (which include in their composition both analog and digital components) of unknown structure are discussed in the report. The algorithm provides considerable reduction of the task dimension by using the knowledge about their designing and constructing rules and it doesn't need increasing of measuring resources.*

The result of the algorithm work is the construct of PCB graphical image which maintain all information necessary for PCB mathematical model building up and automatic generation of in-circuit tests.

Introduction

The suggested algorithm presumes the solution of problems in two levels:

- the identification of an object structure (components' revealing, a location of its place and the identification of electric connections between them) [1];
- the identification of components' types.

The iteration process including the next main steps is realized for it:

- a solution of an upper level problem (after revealing of PCB components and connections between them) brings to a call of a next level problem;
- the initiated problem is solved completely or partially (in the case of absence of a sufficient information at the given stage) and after that a return to an upper level takes place;