

# FPGA TECHNOLOGIES WITH NEURAL NETWORK FOR IMAGE PROCESSING

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## Abstract

One of the promising areas in the field of image processing and analysis is the hardware implementation of neural network for processing and analyzing of images based on FPGA technologies. The structural scheme of the multifunctional calculator was developed. The described structure is a classifier and it is programmed in the FPGA crystal.

**Key words:** FPGA, neural network, image processing.

## Introduction

The main task is to provide processing and analysis of images in real time. Hardware implementation may have a lot of applications: biomedical engineering, aerospace etc. Required time operational characteristics of the system is ensured by parallelism of data and parallel execution of image processing operations. Before image getting to the input of neural network structure is considered image obtained from the camera is preprocessed on a microprocessor. It should accelerate the operation of the device and allow to allocate more memory of FPGA for the classifier.

## Research results

A classifier is programmed in the FPGA crystal whose structure is shown in Fig. 1, which plays a major role, as the result of its functioning is the classification vector.

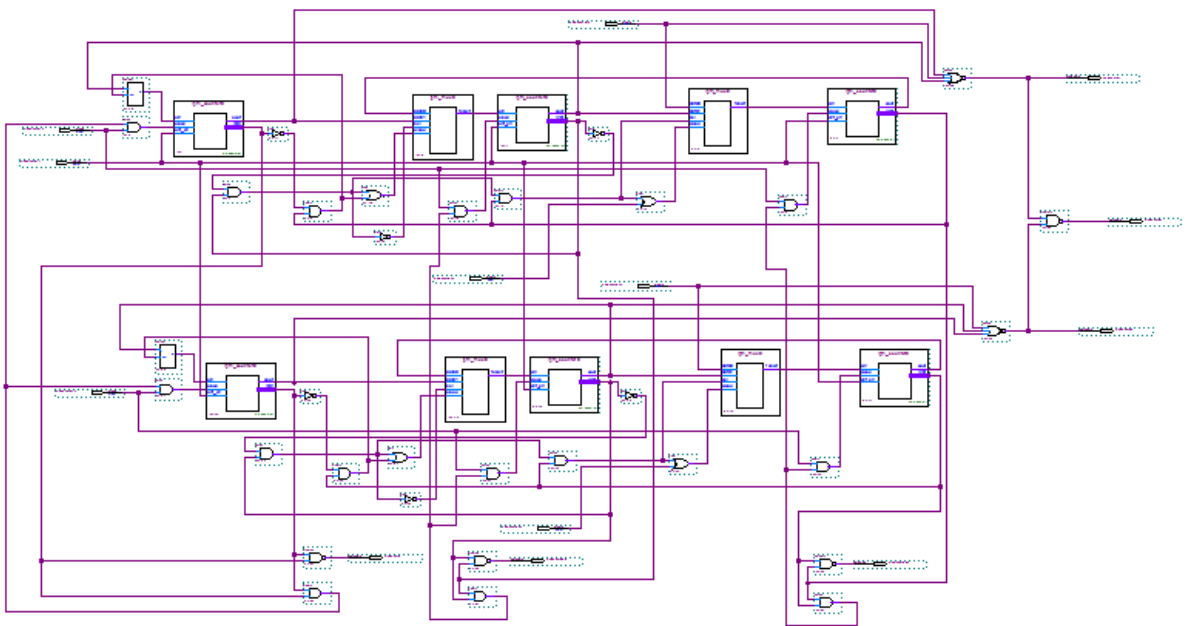


Fig. 1 - Functional scheme of the classifier.

The classifier works in two modes: learning mode (adaptation) and working mode. In the learning mode (adaptation) through the input block the values of the components of the

training vector  $X_k$ , multiplied by the weight coefficients  $w_{ij}$ , are sequentially fed. At the first step, weights  $w_{ij}$  have initial values, and in the process of learning are consistently configurable. In the classification block, the weighted learning signals  $w_{ij} x_i$  are processed, which are fed to its inputs in the form of a matrix of size  $M \times N$ , where  $M$  is the number of classes of images,  $N$  is the dimension of the input vectors.

In future classifier is modified to increase the productivity and processing speed. This can be achieved by increasing the number of logical cells.

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