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## ABSTRACT

The work is devoted to the development of an eight-digit priority encoder constructed on monoimmittance logic gates. The electric circuit on the properties of the long lines in the microwave range was developed. The mathematical model and additional optimization were carried out. The monoimmittance priority encoder computer simulation was performed. The advantages of the developed monoimmittance priority encoder are increased speed, simplicity of design, passive power supply, absence of a threshold of minimum operating voltage and increased immunity to electromagnetic interferences.

**Keywords:** monoimmittance logic gate, combinational logic, priority encoder, passive digital components, microwave computing devices.

## 1. INTRODUCTION

Begin A modern information society requires constant improvement of the computing systems parameters. But, despite the rapid development of semiconductor logic, the theoretical limits for improving their characteristics are limited due to the properties of semiconductor structures, so the question about finding a new physical basis for logical gates arises. At present, directions are being developed to create new logical elements: optical logical elements[1,2], acoustic logic elements[3], spin-diode logic elements[4], microelectromechanical logic elements[5], memristive logic elements[6], quantum logic[7], DNA logic gates[8], magnonic logic circuits[9] and etc.[19-22]. One of possible decisions of the problem is using new functional devices – negatrons [[10]]. Negatrons – devices with negative resistance (R-negatrons), negative capacitance (C-negatrons), and negative inductance (L-negatrons) can be used for construction of logical elements and systems[11-13]. But using active devices leads to increasing power consumption and decreasing noise immunity and reliability. At present, optical, magnetic, radio-frequency and many other types of logic gates are under development. One of them is monoimmittance logic gates, which use as an informative parameter the resistance, inductive or capacitive type of immittances. For today, a full functional basis of monoimmittance logic gates constructed on the basis of transforming properties of long transmission lines in the microwave range is developed[14]. The advantages of such gates are higher speed, passive power supply, absence of the threshold of the minimum operating voltage due to the absence of active elements, and increased immunity to electromagnetic interference due to the use of immittance as an informative parameter[15].

Today, there is a need for the development and research of digital circuits built on the basis of monoimmittance gates. The monoimmittance adder [[16]], half-adder [[17]] and other digital schemes were developed and researched [[14,18]], as well as radio-frequency transponders using monoimmittance logic circuits. The paper considers the minimal functional basis for monoimmittance logic gates and proposes a priority encoder based on them, which converts position code into a binary code, which is presented in the form of immittance logical levels. Such priority encoder is passive and retains all the advantages of monoimmittance logic.

## 2. REVIEW OF THE FUNCTIONAL BASIS OF MONOIMMITTANCE LOGIC GATES

The logical state of the immittance gate is characterized by a resistive immittance value range – «R». For example, logical level – «1» – corresponds to the range of variation $R(1) > R_0$, and logical zero – «0» – corresponds to the range of variation $R(0) < R_0$. Logical gates built on this principle are called monoimmittance. Using as a physical basis the properties of long lines in the microwave range, it is possible to construct a functionally complete basis of

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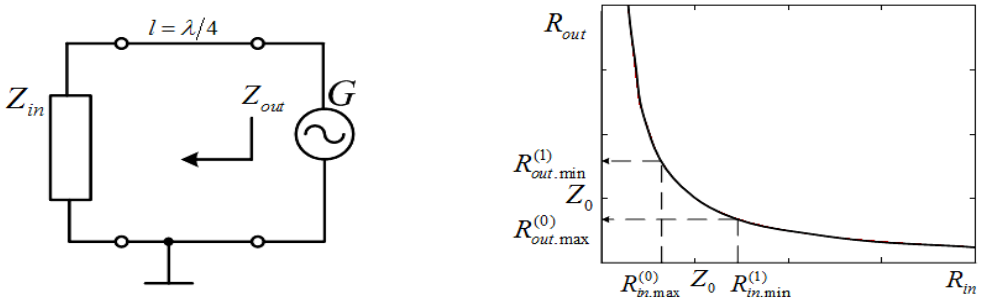
monoimmittance logic gates. This makes it possible to construct combinational schemes based on monoimmittance gates, including the priority encoder. In the following paragraphs, the logical gates necessary for constructing a monoimmittance priority encoder are briefly considered.

### 2.1 Monoimmittance logic R-gate «NOT»

Properties of quarter wave segment of transmission line that realizes "quarter- wave transformer" can be used for implementation of logic function «NOT» (Figure 1a). Output resistance $Z_{out}$ of that kind of segment of the transmission line depends on the resistance $Z_{in}$, which is connected to its input [13]:

$$Z_{out} = Z_0^2 / Z_{in}, \quad (1)$$

where $Z_0$ is the wave impedance of the transmission line.



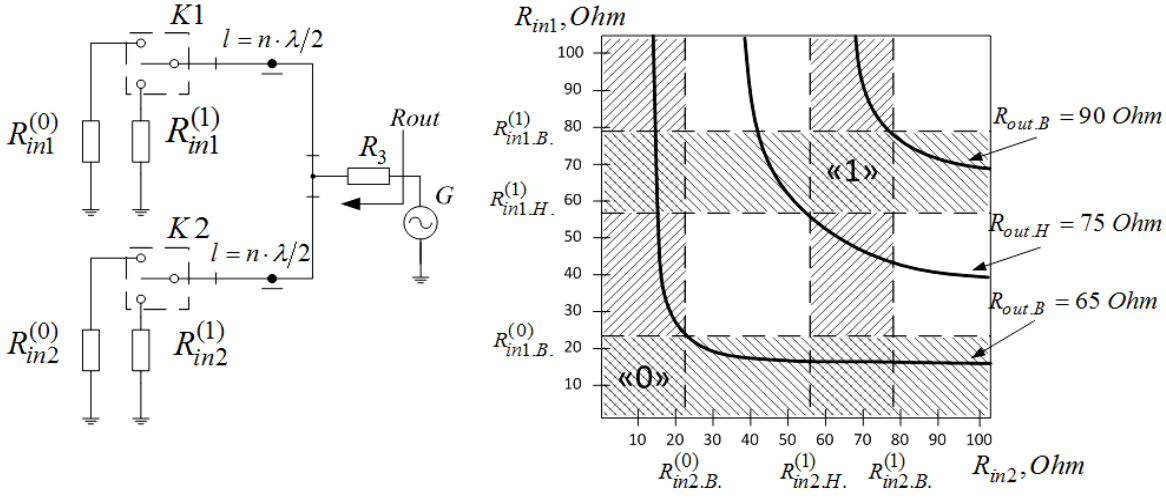

a) b)

Figure 1. "Quarter- wave transformer" (a) that implements monoimmittance logic R-gate "NOT" and its transfer characteristic (b)

If $Z_{in} = R_{in}$, then $Z_{out} = R_{out} = Z_0^2 / R_{in}$. Considering that $Z_0$ is real and fixed the transfer characteristic of the gate has the form shown in Figure 1b. The graph shows that if $R_{in} > Z_0$ then $R_{out} > Z_0$ and conversely. This corresponds to the previously formulated conditions for the monoimmittance logic R-gate "NOT".

### 2.2 Monoimmittance logic R-gate «AND»

The circuit diagram of a possible realization of a monoimmittance logic R-gate «AND» [13] is shown in Figure 2a.




a) b)

Figure 2. The circuit diagram (a) and the immittance transfer characteristic (b) of the monoimmittance logic R-gate “AND” (K1 and K2 – virtual switches)

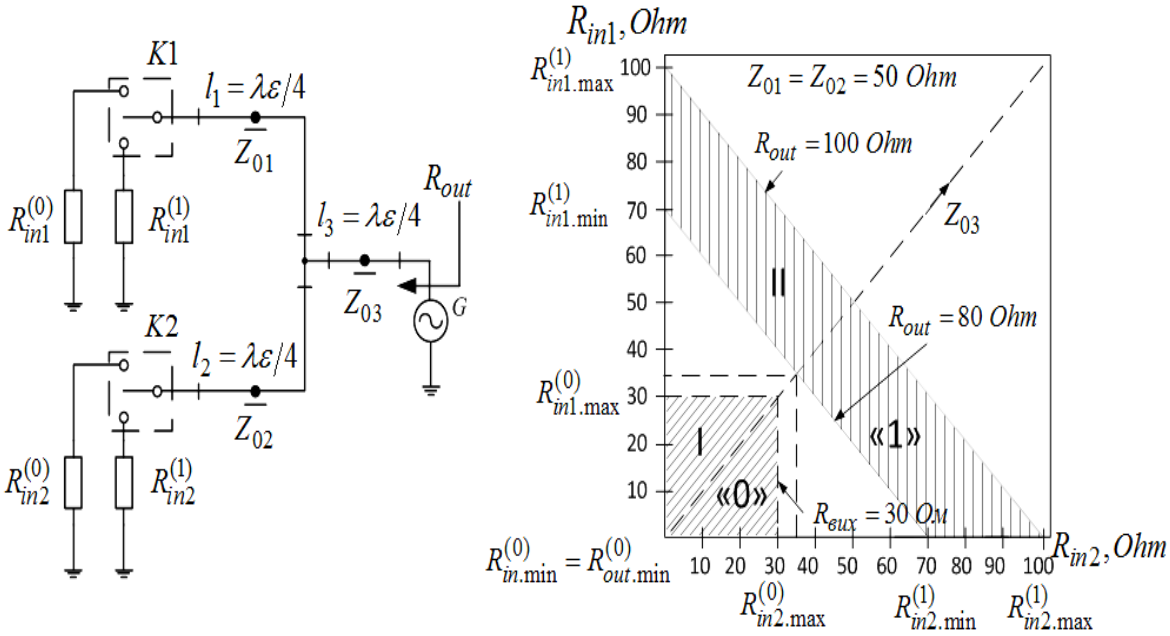
The output circuit resistance, provided in the case that the length of all connecting segments of the transmission line $l = n \cdot \lambda/2$, where $n = 0,1,2...$, $\lambda$ – the length of the electromagnetic wave in the transmission line, is equal to:

$$R_{out} = R_3 + \frac{R_{in1} \cdot R_{in2}}{R_{in1} + R_{in2}}. \quad (2)$$

The equation (2) is a mathematic model of the ideal monoimmittance logic R-gate "AND" and describes its immittance transfer characteristic that is shown in coordinates $R_{in1}$ and $R_{in2}$ as a family of equilateral hyperboles (Figure 2b). The position of the hyperboles can be adjusted by the resistor $R_3$.

### 2.3 Monoimmittance logic R-gate «OR»

The circuit diagram of a possible realization of a monoimmittance logic R-gate "OR" [13] is shown in Figure 3a. The logic gate consists of quarter segments $l_1$, $l_2$, $l_3$ of the transmission line with the characteristic impedance $Z_{01}$, $Z_{02}$, $Z_{03}$ respectively. Resistances $R_{in1}$ and $R_{in2}$ are connected to the logic gate inputs.




a) b)

Figure 3. The circuit diagram (a) and the immittance transfer characteristic (b) of the monoimmittance logic R-gate "OR" (K1 and K2 – virtual switches)

The immittance transfer characteristic of the gate is described by the expression:

$$R_{out} = \frac{Z_{03}^2 \left( Z_{01}^2 R_{in2} + Z_{02}^2 R_{in1} \right)}{Z_{01}^2 \cdot Z_{02}^2}. \quad (3)$$

If we assume that the input channels of the logic gate are the same ( $Z_{01} = Z_{02}$ ) then from (3) we find

$$R_{out} = \frac{Z_{03}^2 \left( R_{in2} + R_{in1} \right)}{Z_{01}^2}. \quad (4)$$

From (4) it is seen that the immittance transfer characteristic of the logic gate in coordinates $R_{in1}$ and $R_{in2}$ plane is a straight line (Figure 3b) which position can be adjusted by selecting the impedances values $Z_{01}$, $Z_{02}$, $Z_{03}$ of segments $l_1$, $l_2$, $l_3$ of the transmission line.

The logical gates considered above constitute a complete functional basis, on which all other logical gates and combinational schemes can be constructed.

## 3. DEVELOPMENT AND RESEARCH OF A MONOIMMITTANCE PRIORITY ENCODER

On the basis of the monoimmittance gates mentioned above, a monoimmittance priority encoder was constructed. If the resistance is used as an informative parameter, the truth table for the monoimmittance priority encoder will have the form shown in Table 1.

Table 1 – The truth table of a monoimmittance priority encoder

| $R_{in1}$ | $R_{in2}$ | $R_{in3}$ | $R_{in4}$ | $R_{in5}$ | $R_{in6}$ | $R_{in7}$ | $R_{out1}$ | $R_{out2}$ | $R_{out3}$ |
|---|---|---|---|---|---|---|---|---|---|
| «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ |
| «1» $R > Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «1» $R > Z_0$ |
| X | «1» $R > Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «1» $R > Z_0$ | «0» $R < Z_0$ |
| X | X | «1» $R > Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «1» $R > Z_0$ | «1» $R > Z_0$ |
| X | X | X | «1» $R > Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «1» $R > Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ |
| X | X | X | X | «1» $R > Z_0$ | «0» $R < Z_0$ | «0» $R < Z_0$ | «1» $R > Z_0$ | «0» $R < Z_0$ | «1» $R > Z_0$ |
| X | X | X | X | X | «1» $R > Z_0$ | «0» $R < Z_0$ | «1» $R > Z_0$ | «1» $R > Z_0$ | «0» $R < Z_0$ |
| X | X | X | X | X | X | «1» $R > Z_0$ | «1» $R > Z_0$ | «1» $R > Z_0$ | «1» $R > Z_0$ |

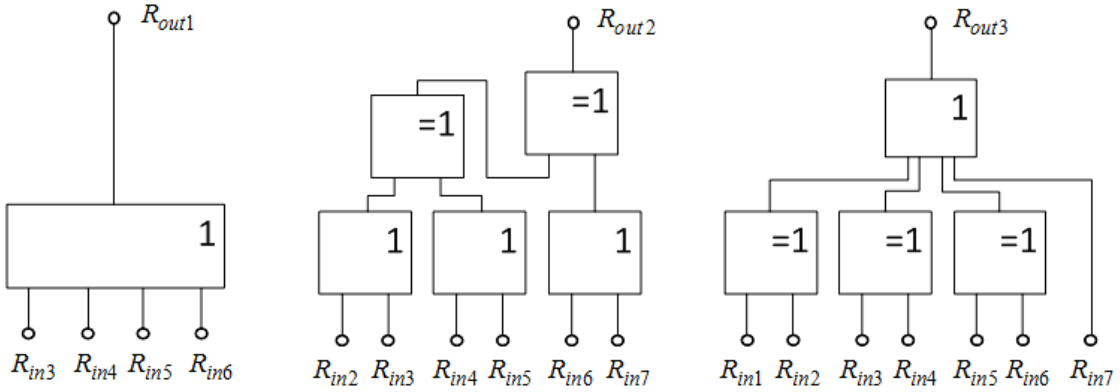



Figure 4. Structural scheme of the monoimmittance priority encoder

A possible construction variant of such encoder is presented in the form of a structural scheme in Figure 4:

To simplify the scheme, it is possible to replace the modulo-2 adder with the logic gate that performs the function of inversion of direct implication. Also due to the properties of the transmission line segments, additional optimization of

the scheme has been carried out. Thus, the scheme of the priority encoder, constructed on monoimmittance logic gates, is shown in Figure 5:

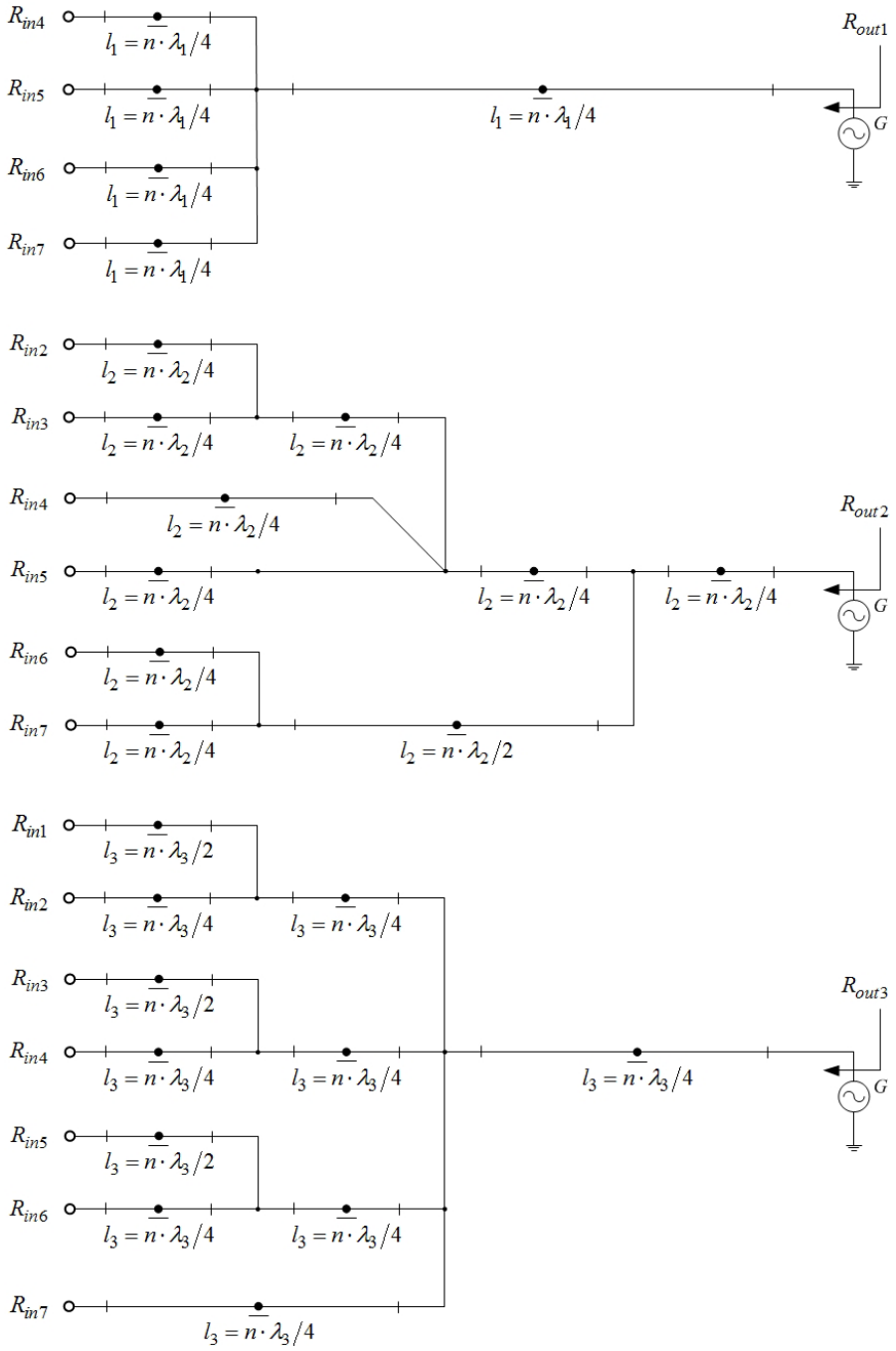



Figure 5. The monoimmittance priority encoder scheme

With the help of mathematical models of monoimmittance gates, the mathematical model of the monoimmittance priority encoder is obtained, which, for convenience of presentation, is divided into parts. The immittance of the first encoder output is:

$$R_{out1} = \frac{Z_0^2}{\frac{R_1 \cdot R_2 \cdot R_3 \cdot R_4}{R_2 \cdot R_3 \cdot R_4 + R_1 \cdot R_3 \cdot R_4 + R_1 \cdot R_2 \cdot R_4 + R_1 \cdot R_2 \cdot R_3}}, \quad (5)$$

where

$$R_1 = \frac{Z_0^2}{\frac{R_{in1} \cdot Z_0^2 / R_{in2}}{R_{in1} + Z_0^2 / R_{in2}}}, \; R_2 = \frac{Z_0^2}{\frac{R_{in3} \cdot Z_0^2 / R_{in4}}{R_{in3} + Z_0^2 / R_{in4}}}, \; R_3 = \frac{Z_0^2}{\frac{R_{in5} \cdot Z_0^2 / R_{in6}}{R_{in5} + Z_0^2 / R_{in6}}}, \; R_4 = \frac{Z_0^2}{R_{in7}}.$$

The immittance of the second encoder output is:

$$R_{out2} = \frac{Z_0^2}{\frac{R_3 \cdot Z_0^2 \Big/ \frac{R_1 \cdot R_2}{R_1 + R_2}}{R_3 \cdot Z_0^2 \Big/ \frac{R_1 \cdot R_2}{R_1 + R_2}}}, \quad (6)$$

where

$$R_1 = \frac{Z_0^2}{\frac{Z_0^2 / R_{in2} \cdot Z_0^2 / R_{in3}}{Z_0^2 / R_{in2} + Z_0^2 / R_{in3}}}, \; R_2 = \frac{Z_0^2 / R_{in4} \cdot Z_0^2 / R_{in5}}{Z_0^2 / R_{in4} + Z_0^2 / R_{in5}}, \; R_3 = \frac{Z_0^2 / R_{in6} \cdot Z_0^2 / R_{in7}}{Z_0^2 / R_{in6} + Z_0^2 / R_{in7}}.$$

The immittance of the third encoder output is:

$$R_{out3} = \frac{Z_0^2}{\frac{Z_0^2 / R_{in4} \cdot Z_0^2 / R_{in5} \cdot Z_0^2 / R_{in6} \cdot Z_0^2 / R_{in7}}{\frac{Z_0^2}{R_{in5}} \cdot \frac{Z_0^2}{R_{in6}} \cdot \frac{Z_0^2}{R_{in7}} + \frac{Z_0^2}{R_{in4}} \cdot \frac{Z_0^2}{R_{in6}} \cdot \frac{Z_0^2}{R_{in7}} + \frac{Z_0^2}{R_{in4}} \cdot \frac{Z_0^2}{R_{in5}} \cdot \frac{Z_0^2}{R_{in7}} + \frac{Z_0^2}{R_{in4}} \cdot \frac{Z_0^2}{R_{in5}} \cdot \frac{Z_0^2}{R_{in6}}}}. \quad (7)$$

The proposed mathematical models are based on the condition that the wave resistance $Z_0$ of all segments of the transmission line is the same.

With the help of mathematical models (5-7) the transfer characteristic of the monoimmittance priority encoder was modeled (Figure 6), and for the simulation of the logical "1" the input terminal resistance of 150 Ohms was chosen, and for the logic "0" the resistance of 5 Ohms was chosen.

From the graph in Fig. 6, we can see that the output impedance of the logical "0" does not exceed 20 Ohms, and the output impedance of the logical "1" is not less than 105 Ohms. The received transmission characteristics confirm the correspondence of the monoimmittance priority encoder functioning to the truth table given in Table 1.

Let's calculate the speed of the monoimmittance priority encoder. For the scheme of the monoimmittance logical R-gate "NOT", realized on the basis of a microstrip line with a dielectric filling, on condition $l = \lambda/4$, $\mu = 1$, time of electric signal passing is equal:

$$\tau(NOT) = \sqrt{\varepsilon}/4f. \quad (5)$$

For the monoimmittance priority encoder, the maximum length of the passage of an electric signal is equal to length of 4 monoimmittance logic gates «NOT»:

$$\tau(PE) = \sqrt{\varepsilon}/f \quad (6)$$

When using a ceramic dielectric substrate with $\varepsilon = 9$ at frequency 10GHz the potential delay time is $\tau(PE) = 300$ ps. When using an air dielectric with $\varepsilon = 1$, we have $\tau(PE) = 100$ ps. When the carrier frequency is increased to 100GHz the speed of the monoimmittance priority encoder is equal to 30ps and 10ps respectively.

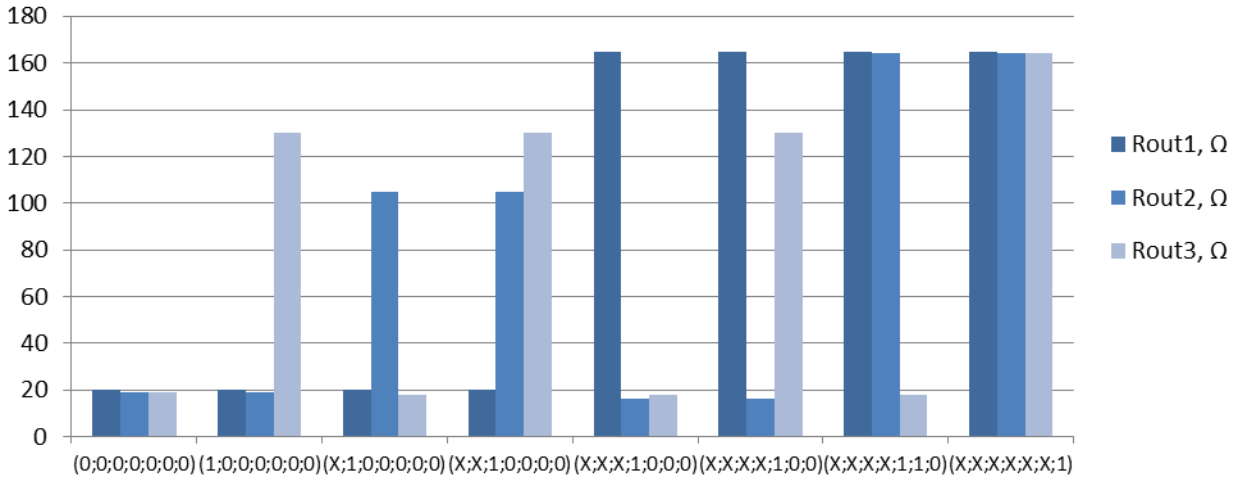



Figure 6. Transmission characteristics of the monoimmittance priority encoder

Due to the absence of active elements in the circuit, the monoimmittance priority encoder does not require constant power supply, because it is powered by an informative UHF signal, and does not have a threshold of minimum operating voltage. Because all the immittance transformations occur with the properties of the quarter-wave and half-wave segments of the microstrip line, the design and manufacturing technology of the developed monoimmittance priority encoder is very simple. Also, the use of immittance as an informative parameter gives a high immunity to electromagnetic interference, since the noise and voltage surges in the electric circuit do not change the value of the input and output immittances, as well as the wave resistance of the transmission line segments.

## 4. CONCLUSIONS

The monoimmittance priority encoder, built on the quarter-wave and half-wave segments of the transmission line, is proposed in paper. An electrical scheme was developed, which, due to the properties of the transmission line, was further optimized, and a mathematical model was proposed, by means of which the transfer characteristic of the monoimmittance priority encoder was calculated. The results of the calculations revealed that the functioning of the proposed device corresponds to the truth table of the priority encoder. The monoimmittance priority encoder retains all the advantages of monoimmittance logic gates, such as high speed (which can reach 10 ps in certain conditions), simplicity of design, passive power supply, absence of a threshold of minimum operating voltage and increased immunity to electromagnetic interferences. Such encoder can be used in passive computing systems, as well as in systems that operate under high electromagnetic interferences, and can be used to build, for example, an analog-to-digital converter.

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