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DESIGN AND SIMULATION OF CONTINUOUSLY LOGICAL ANALOG-TO-DIGITAL CONVERTERS WITH ADCANCED FUNCTIONS FOR IMAGE PROCESSORS

Abstract. *The paper considers results of design and modeling of continuously logical analog-to-digital converters (CL_ADC) based on current mirrors (CM) with advanced functions of preliminary analogue and subsequent processing for creating sensor multi-channel analog-to-digital converters (SMC ADCs) and image processors (IP). For such with parallel inputs-outputs IP and SMC ADCs it is needed active photosensitive basic cells (BC) with an extended electronic circuit, which are considered in paper. Such BCs and ADCs based on them have a number of advantages: high speed and reliability, simplicity, small power consumption, high integration level for linear and matrix structures. We show design of the BC and CL_ADC of photocurrents and their possible implementations and its simulations. We consider CL_ADC with conversion to binary codes and Gray codes. Each channel of the structure consists of several digital-analog cells (DC) on 15-35 CMOS. The amount of DC does not exceed the number of digits of the formed code, and for an iteration type, only one cell of DC, complemented by the device of selection and holding (SHD), is required. One channel of CL_ADC with iteration is based on one DC-(G) and SHD, and it has only 35 CMOS transistors. In such ADCs easily parallel code can be realized and also serial-parallel output code. The circuits and simulation results of their design with OrCAD are shown. The supply voltage of the DC is 1.8÷3.3V, the range of an input photocurrent is 0.1÷24μA, the transformation time is 20÷30nS at 6-8 bit binary or Gray codes. The general power consumption of the ADC with iteration is only 50÷100μW, if the maximum input current is 4μA. Such simple structure of linear array of ADCs with low power consumption and supply voltage 3.3V, and at the same time with good dynamic characteristics (frequency of digitization even for 1.5μm CMOS-technologies is 40÷50 MHz, and can be increased up to 10 times) and accuracy characteristics are show. The CL_ADCs opens new prospects for realization of photo-electronic structures and IP with matrix operands, which are necessary for neural networks, digital processors fuzzy controllers.*

Introduction. Too slow and too few interconnects between VLSI circuits cause a bottleneck in the communication between processor and memory or processors. The problem is getting worse since the increasing integration density of devices leads to a higher requirement in the number of necessary channels for the off-chip communication. The use of optical interconnects is discussed as an alternative to solve the mentioned problems on interconnect in VLSI technology. A lot of demonstrator systems were built to prove the use of optics or optoelectronics for off-chip and on-chip interconnects. In OE-VLSI one tries to solve limitation problem by realizing external interconnects not at the edge of a chip but with arrays of optical detectors and light emitters which send and receive data directly out from the chip area. This allows the realization of stacked 3-D chip architecture in principle [1]. At present the situation for smart detector circuits is much easier. They can be regarded as a subset of OE-VLSI circuits because they consist only of arrays of photo-detectors with corresponding evaluation circuit for analogue to digital converting. Optical detectors based on photodiodes can be monolithically integrated with digital electronics in silicon, which significantly simplifies design of OE-VLSI circuits, which in addition should contain only light-emitting devices. Furthermore smart detector circuits can be manufactured in nearly every semiconductor fabric. Smart optical sensors [2, 3] show a great application field and market potential. Therefore our approach favors smart pixel like architecture combining parallel signal detection with parallel signal processing in one circuit. Each pixel has its own analog and analog-digit node what guarantees the fastest processing. The strategic direction of solution of various scientific problems becomes fast-acting and parallel processing of 2D data large arrays using non-conventional computational MIMO-systems, corresponding matrix logics (ML) (multi-valued, signed-digit, fuzzy logics, continuous, neural-fuzzy and others) and corresponding mathematical apparatus [4-7]. For realizations of optical learning neural networks (NN) with 2D structure [4, 8-10], of the continuous logic equivalency models (CLEM) NN [5, 8, 9], the elements of matrix logic are required, and not only of two-valued, but also continuous, threshold logics [5-7]. The adequate structure of vector-matrix computational procedures with basic operations of above-mentioned logics, are required. Advanced non-traditional parallel computing structures

and MIMO-systems [3], require both parallel processing and parallel inputs/outputs. In article [11] mathematical foundations of the universal (multifunctional) logic elements (ULE) of the ML design with fast programmable tuning are considered, where the expediency of functional basis unification and the need for ADC [12] arrays and storage (matrix type) has been shown. ADC is continuously-discrete automaton, which is carrying out transformation of analogue size x by its interaction with standard in sizes in a discrete output code. Aspects of the theory and designing practice and use ADC and DAC are so widely stated, what even it is difficult to choose the most generalizing works. Certain successes are attained in area of creation of 2D devices of ML, 2D storages for such parallel informatively-measuring systems and digital optoelectronic processors (DOEPs). "Bottleneck" in parallel DOEP is ADC, which unlike traditional systems of input with scanning or series-parallel reading and output, should make in parallel completely ADC considerable quantity transformation (256 x 256 and more) signals and to provide rate of input, up to 10^6-10^7 frames per second. Therefore only creation SMC_ADC images with multi parallel inputs and outputs, i.e. ADC with vector or matrix organization (VMO) [12-14], which all channels work in parallel and provide (low power consumption, simple circuit realization, small time of transformation, low levels of the entrance signals, comprehensible word length and i.e.), the above-stated problems can solve . Besides, such ADC VMO also can carry out and other functions, for example, calculation of logic operations over matrixes, a digital filtration and digital addition-subtraction of images. In papers [13, 14] equivalently (EQ) continuously logical (CL) ADC which allows to obtaining high performance with smaller amounts of equipment were considered. Such ADC consist of n serially connected digital-analog cells (DCs), implementing CL - functions and built in CMOS-transistors with a current-mode operation. The selection of the required continuously-logical functions for analog-to-digital conversion and corresponding ABC circuits influences on parameters and performance of such CL_ADC, including the output codes. An amount of channels in multichannel converters for the optical parallel and multisensory systems is considerable. **Formulation of the problem and goal of the work.** Therefore for such applications digit-by-digit serial-parallel arrays are more preferable. Consequently, the aim of our work is design and modeling ADC and their of CL DCs based on CM with functions of preliminary analogue and subsequent analogue-digital processing for creating sensor multi-channel analog-to-digital converters (SMC ADCs) and image processors (IP). In addition, in our previous works, the accuracy characteristics of the ADC were not considered, no estimates of conversion errors were made for different possible modes and modifications of such CL DCs and ADCs as a whole. That is why the purpose of the present work is also to evaluate ADC errors, demonstrate them by specific experimental results, and also further enhancements of such ADCs and their basic cells, which significantly expand their functionality and the range of problems they solve.

Research results. 1. Basic foundations, equivalence models for SMC_CL_ADC.

The CL – transformations are shown in papers [13], in which the transformation CL functions (CLF) are defined and it is shown that the operation of min, max of CL are the basic operations of the functions. Use of operators of hybrid logic it is possible: $D_1[P(x1,x2)] = \max(x_1,x_2)$, $D_2[P(x1,x2)] = \min(x_1,x_2)$, where P and D are respectively the threshold and the de-threshold operators, which are realized by various means. In many NN models for recognition of images, especially a lot of graded, it is desirable to have picture binary bit-planes, which encode the image matrix in Gray codes. Besides, in a number of works [5-9] it has been shown that some operations of continuous logic, such as equivalence and nonequivalence, and their generalized family. These scalar operations of equivalence eq(x,y) and nonequivalence neq(x,y) for x,y $\in$[0,1] are defined in works [5, 13, 14] namely: eq (x, y) = $x \wedge y + \bar{x} \wedge \bar{y} = \min(x,y) + \min((1-x),(1-y)) = 1 - |x-y|$,

neq(x,y)= $|x-y| = 1 - eq(x,y) = = \max(x,y) - \min(x,y) = \max(\bar{x},\bar{y}) - \min(\bar{x},\bar{y}) = (x \dot{-} y) + (y \dot{-} x)$,

where $(\dot{-})$ - is the operation of a limited difference. If we consider that at y = $1 \dot{-} x = \bar{x}$, these functions are transformed to: eq(x, $\bar{x}$) = 2(x $\wedge$ $\bar{x}$) = 2min(x, $\bar{x}$), neq(x, $\bar{x}$) = max(x, $\bar{x}$) - min(x, $\bar{x}$) = 1-2min(x, $\bar{x}$), as has been shown in works [13], these functions can be successfully used in CL_ADC. For formation of binary bit-planes which answer picture categories of a Gray code, we used per pixel iterative procedure over matrixes of equivalence and nonequivalence of signals or equivalence and nonequivalence, received on the previous steps: $eq_{i+1}(eq_i(\dots),neq_i(\dots))$ and $neq_{i+1}(eq_i(\dots),neq_i(\dots))$. It is easy to notice that splitting of a piece [0, 1] on $2^n = N$ sub-bands, puts to each of them a set, a vector of signs which corresponds to a code Gray, the measured scalar size x. Thus, positional digit d_{n-i} of code is de-

fined $d_{n-i}(eq_{i-1}, neq_{i-1}) = \{1, \text{ if } eq_{i-1} > neq_{i-1}, 0, \text{ if else}\}$, where $i \in 1 \div n$, $eq_0 = x$, $neq_0 = \bar{x}$. From here evidently, that for realization ADC of optical signals, we needed to synthesize the CL BCs, which realize demanded operations eq_i, neq_i and the threshold operators. We name such ADC equivalently continuous-logic complementary-dual, as in them signals x and $\bar{x}$ are complementary and functions CL are equivalence (nonequivalence), i.e. equivalently CL_ADC [13]. Since these ADC were implemented on the current mirrors (CM), and input signals of ADC are currents, then we shall denote such ADC as ADC CM. In this work as transformation CLFs we use the following functions: $eq_{i+1}(eq_i, D/2) = 2(eq_i \dot{-} 2(eq_i \dot{-} D/2))$or $neq_{i+1}(neq_i, D/2) = 2|neq_i - D/2|$, where $eq_0 = x$, $neq_0 = \bar{x}$, which allow us to work not with two signals, but with 1 signal, thereby simplifying the implementation of DCs. The SMC_ADC for IP is shown in Fig. 1.

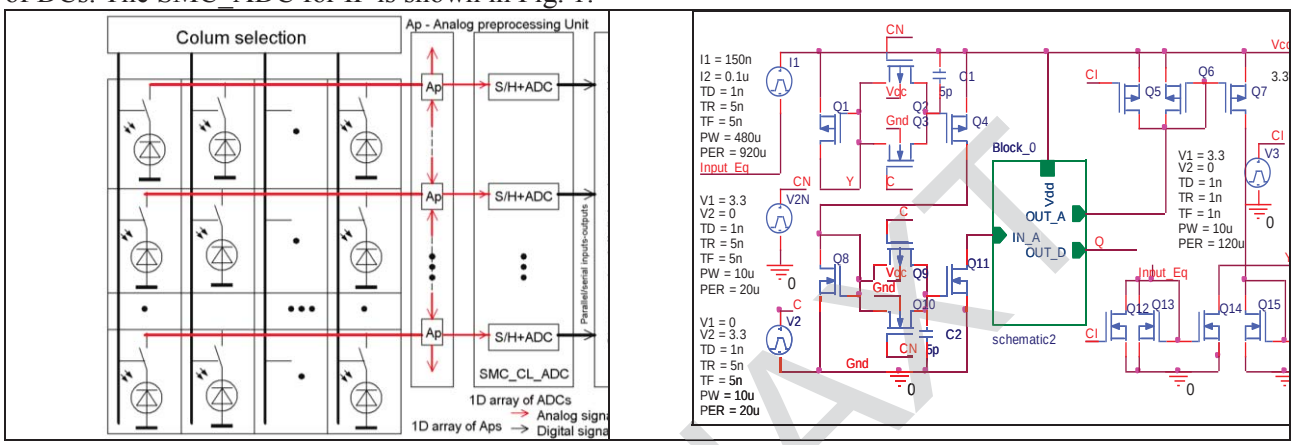
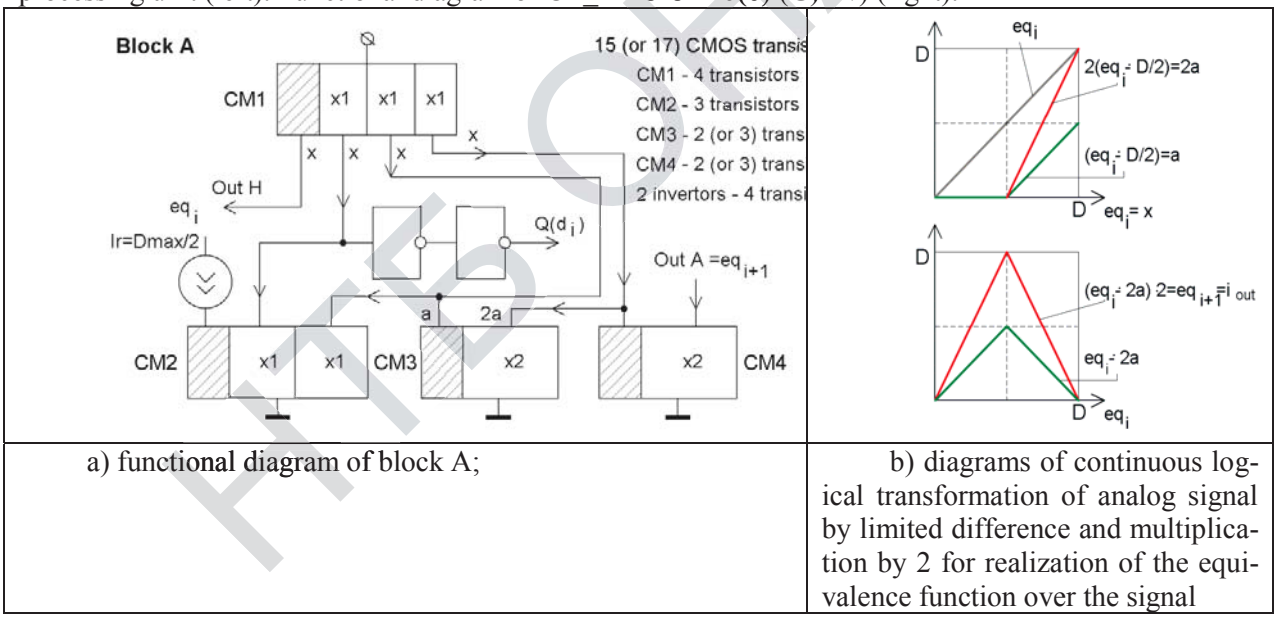


Fig. 1. Structure of 2D image sensor with 1D array of CL_ADC and storage or/and digital codes processing unit (left). Functional diagram of CL_ADC CM-6(8) (G) -iv) (right).



a) functional diagram of block A;

b) diagrams of continuous logical transformation of analog signal by limited difference and multiplication by 2 for realization of the equivalence function over the signal

Fig. 2. Circuits of the one channel of multichannel CL_ADC CM-6(8) (G) -iv with iteration transformation and base cell DC-(G)

2. Design of CL ADC CM-6(8) (G) -iv (the iteration variant) on DC-(G) (with Gray code) with Orcad.

Circuit of the one channel of SMC_ ADC is shown in Fig.1. The circuit is based on one digital-analog cells DC-(G) (Block A), devices of selection and holding (SHD) and additional elements (Block B). The block A or (DC) is shown in Fig. 2a. Essence of the circuit is in that input analog current signal, subject to transformation, is written to SHD, and than given to analog DC-(G), which will form the next digital bit of output code and CL function which in future will be again given on SHD for forming next successive bits. DC - (G) consists of 15 or 17 transistors (Ts) and current generator. Device of SHD is based on 18 transistors. Thus complication of the circuit of one channel is 33 (35) transistors, which do it perspective for wireless multisensory systems. The DC converts the input signal to another output current

signal, using CLF (section 1) over currents and simultaneously compares it with the threshold current. Thus, there is a wide choice for searching and optimizing such DCs taking into account the required goal. To minimize the hardware costs, cells can be very simple and consist of 10-20 Ts. The advantage of a structure with a serial output of the Gray code is that increasing the number of iterations increases the bit ADC with an unchanged structure. To convert a serial Gray code to a binary code, only one modulo adder and one D flip-flop are required. In Figures 3 the results of simulation of one channel of six bits CL_ADC CM-6 (G) -iv) at linear-increasing input currents are shown. The total power consumption of this ADC-6 (8) (G) -iv did not exceed 70μW with a maximum input current of 4 μA and a conversion period of 120μS (6x20 μS for 6 bits) and 160μS (8x20 μS for 8 bits). For modes with lower currents and Vdd = 1.5 ÷ 1.8V, the power consumption of ADC-6 (8) can be reduced to 10 ÷ 15μW.

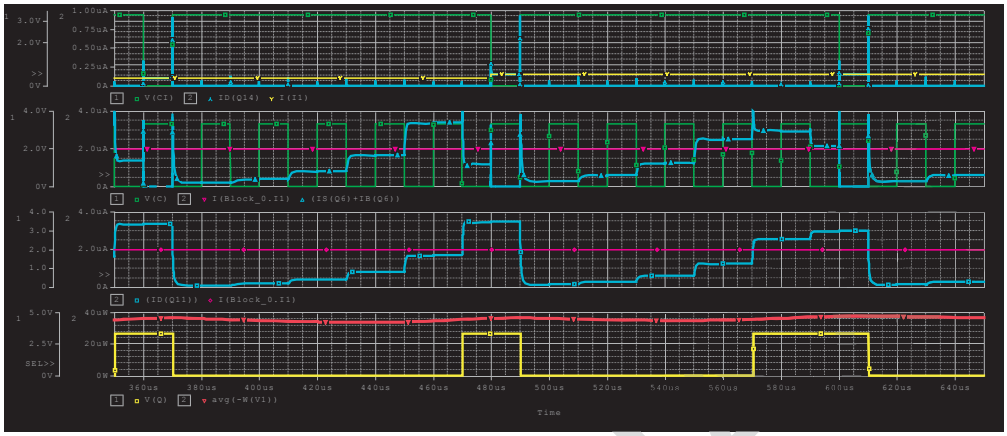


Fig. 3. a) Simulation result for two input currents 100nA and 150nA, corresponding output Gray codes {000001} and {000011}; the blue line in the third trace is output current of the block for six digits ADC, the violet line is the threshold current; the yellow line in the fourth trace is output voltage of the block that corresponds to output code (a time interval for the first code 370μs - 490 μs (six digits by 20 μs), a time interval for the second code 490μs - 610 μs; the red line is the consumption power about 40μW

The simulation results and diagrams, under other modes and currents, will be presented in the report. They confirm the correct functioning of the proposed ADC. The drawback of our earlier works is the lack of research on the ultimate capabilities of such structures and their precision characteristics. Therefore, in this paper, we pre-observed such a structure in the formation of eight digit code, determined the possibility of operation with very small input currents (10nA ÷ 1μA), and adding to the structure of the DAC and converters from the Gray code to the binary code (see Fig. 4 and Fig. 5 with parallel outputs), determined the magnitude of ADC errors and its accuracy characteristics. At the decline of requirements to the fast-acting the offered chart allows using the analog-digital transformations for less amplitude input currents and, power consumption of such one channel of ADC can be less than 50μW for Dmax=1μA. All shown circuits are simulated on 1.5 μm CMOS Ts. Analog-to-digital conversion errors simulation is shown in Fig. 6. The simulation is done for Dmax=4μA, 6-bit ADC, conversion period T=120 μs. As shown in the Fig. 6 the maximal error is about 1 least significant bit (LSB), and only for maximal input current is about 2 LSB for 8-bit ADC. In Fig. 4 diagram of CL_ADC CM-(8) (G) - iv with Gray-to-binary code transformation and serial/parallel outputs with code converter and DAC for errors calculation are shown. Actually the ADC itself, from which 1D or 2D arrays will be done for sensors or image processors, in contrast to the circuit in Fig. 2 may additionally comprise some digital elements, for example, a logic element and a trigger or register. This depends on the possible modes and requirements regarding the formats of output and storage of code arrays. Therefore, in Fig. 4, these additional optional units are marked with a dash-dotted line. And to test the accuracy and timing characteristics in the dynamics, we used two registers and DAC. The results of modeling this circuit are partially shown in Fig. 6 and confirm the correct operation and analog-to-digital and code conversion, both when linearly increasing (decreasing) and sinusoidal current signals are applied to the ADC input. They show that for the 8-bit ADC, even in high-speed (Imax to 16 ÷ 24μA) and low-voltage low-frequency energy-efficient modes (with Imax, namely 1μA, 4μA), the maximum error does not exceed 4 ÷ 5 quantization quanta, and the average error does not exceed 2 LSB. The simulations results CL_ADC with a parallel-serial output have shown, that in such parallel-conveyor CL_ADC (P_C) 6 (8)-DC-(G) at change Imax from 16μA to 24μA the consumption power at 3,3 V was from 1μW to 2μW(6 bits) and

3μW(8 bits). The conversion frequencies in the experiments were for these currents: 32, 40, 50 MHz for 16μA and 64 MHz for 24μA and 40μA. They correspond to different regimes: different Imax, namely 1μA, 4μA, 16μA, 24μA, 40μA; various 1,5V, 1,8V, 2,5V, 3,3V; various transformation periods T (0,02μS, 0,025μS, 1μS, 20μS, 100μS) etc. These researches show, that power consumption actually ADC for the specified values Imax (equal 1μA and 1,8V, 64nA and 1,5V) makes accordingly 40μW and 2μW, tht quantization step is 15,625nA for Imax=4μA and 62.5nA for Imax=16μA, and quantization frequency 40 MHz.

Conclusions. Thus we offered variants of realization of digital-analog cells (DC) and structures of CL ADC CM on their basis. It is shown that such ADC have simplicity, because the amount of DCs does not exceed the number of digits of the formed code, and for an iteration type, only one DC, complemented by the device of selection and holding, is required. In such ADC easily parallel code can be realized and also serial-parallel output code. The circuits and simulation results of their design with OrCAD are shown.

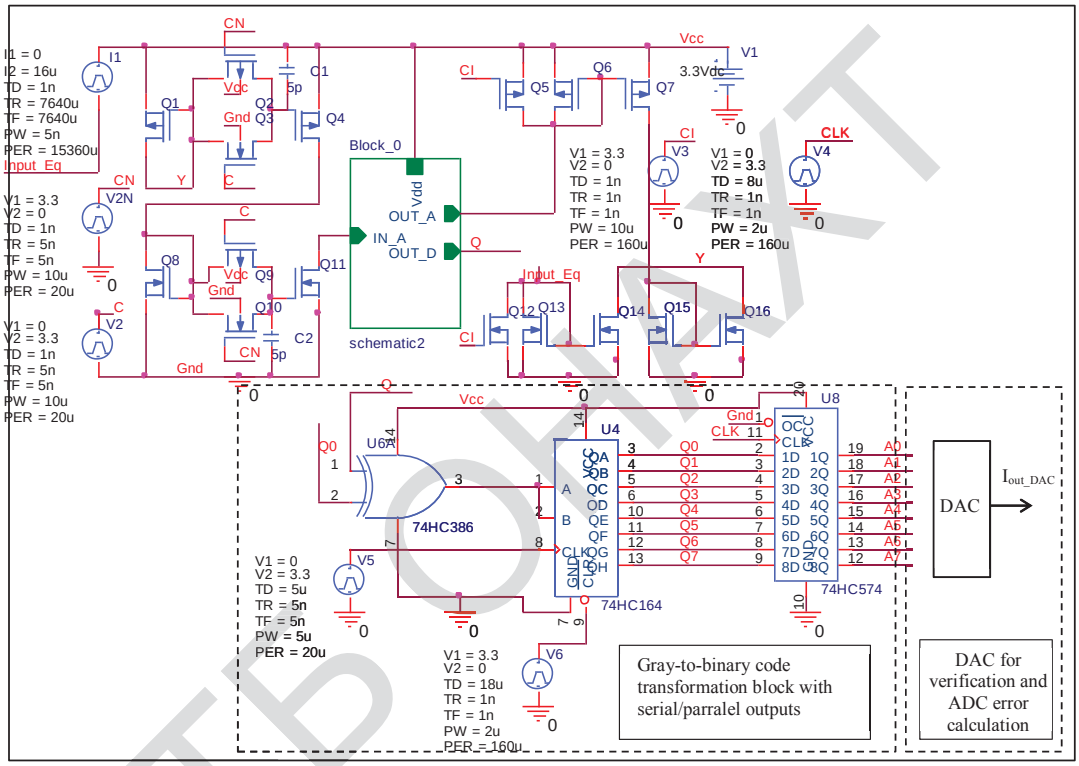


Fig. 4. Functional diagram of CL_ADC CM-(8) (G) -iv) with Gray-to-binary code transformation and serial/parallel outputs with code converter and DAC for errors calculation.

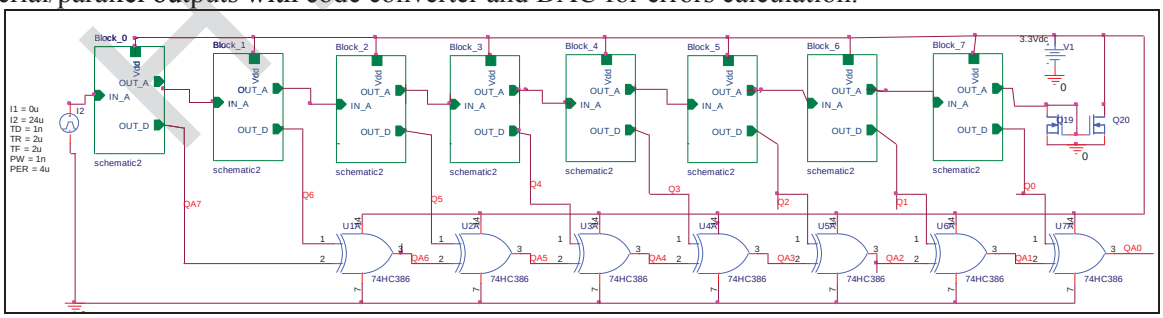


Fig. 5. Structure of 8 bit ADC: a) with Gray code parallel outputs (Q0-Q7); b) with Gray-to-binary code transformation and parallel outputs (QA0-QA7)

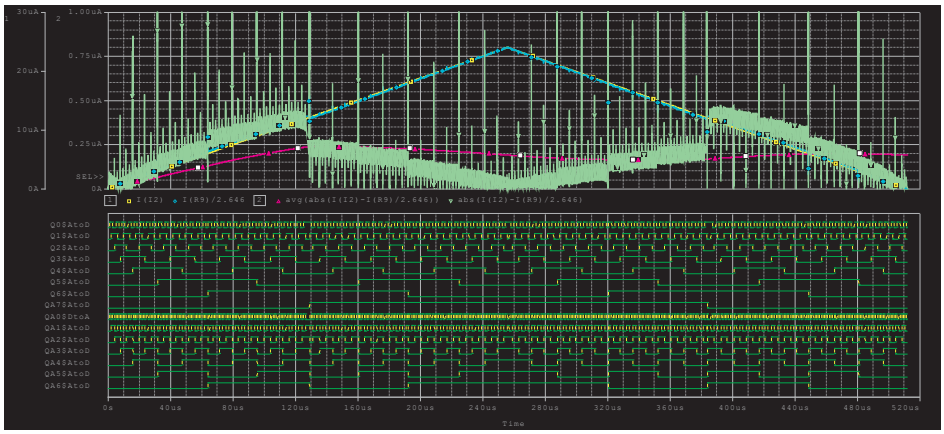


Fig. 6. Time diagrams of 8 bit parallel CL_ADC signals by simulation for I_{input_max}=24μA, ADC conversion time is 1μs; the blue line is the DAC output current, the yellow line is the ADC input current, the violet line is the average ADC current error (<250nA), the green line is the ADC current error; QA0-QA7 – output digital signals of binary parallel code, Q0..Q7 (Q7=QA7) – output digital signals of Gray parallel code

Conclusions (continuation). Such simple CL_ADC CM with low power consumption ≤3mW and supply voltage 1.8÷3.3V, and at the same time with good dynamic characteristics (frequency of digitization even for 1,5μm CMOS-technologies is 40MHz, and can be increased up to 10 times) and accuracy (Δ quantization=15.6÷62.5nA for Imax=4÷16μA) characteristics are shown. The range of optical signals, taking into account sensitivity of modern photo-detectors, can be 1-200 μW. One channel of the ADC with iteration is based on one DC-(G) and SHD, and it has only 35÷40 CMOS transistors. Since such 1D, 2D arrays of serial ADCs are very perspective for sensors and IP. The general power consumption of one ADC, in this case, is only 50÷70μW, if the maximum input current is 4μA. For high performance and frequency of conversions, it is preferable to use the parallel-pipeline CL_ADC (P_C) scheme based on the set of 8-DC-(G) with parallel-serial outputs. The maximal error is about 1 LSB, and only for maximal input current is about 2 LSB for 8-bit CL_ADC.

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XI МІЖНАРОДНА НАУКОВО-ПРАКТИЧНА КОНФЕРЕНЦІЯ

ІНФОРМАЦІЙНІ ТЕХНОЛОГІЇ І АВТОМАТИЗАЦІЯ – 2018

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4 – 5 ЖОВТНЯ, 2018

Збірник включає доповіді учасників XI Міжнародної науково-практичної конференції «Інформаційні технології і автоматизація – 2018»

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