Oleg Sergiyenko · Wendy Flores-Fuentes · Paolo Mercorelli *Editors*

Machine Vision and Navigation

This book presents a variety of perspectives on vision-based applications. These contributions are focused on optoelectronic sensors, 3D & 2D machine vision technologies, robot navigation, control schemes, motion controllers, intelligent algorithms and vision systems. The authors focus on applications of unmanned aerial vehicles, autonomous and mobile robots, industrial inspection applications and structural health monitoring. Recent advanced research in measurement and others areas where 3D & 2D machine vision and machine control play an important role, as well as surveys and reviews about vision-based applications. These topics are of interest to readers from diverse areas, including electrical, electronics and computer engineering, technologists, students and non-specialist readers.

- Presents current research in image and signal sensors, methods, and 3D & 2D technologies in vision-based theories and applications;
- Discusses applications such as daily use devices including robotics, detection, tracking and stereoscopic vision systems, pose estimation, avoidance of objects, control and data exchange for navigation, and aerial imagery processing;
- Includes research contributions in scientific, industrial, and civil applications.

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Preface

Machine vision to provide spatial coordinate's measurement has developed in a wide range of technologies for multiple fields of applications such as robot navigation, medical scanning, and structural health monitoring, to mention some. Machine vision methods also have applications in search, classification, industrial process robotics (monitoring tools capable of visualizing various phenomena that occur during industrial process), rescue, vigilance, mapping, dangerous objects/subjects detection, and other areas where machine control based on vision plays an important role. The computer vision has guided the machine vision to the tendency of duplicating the abilities of human vision by electronically perceiving and understanding an image for high-dimensional data and optimizing the data storage requirement and the time processing due to the complexity of algorithms to extract important patterns and trends to understand what data says.

Autonomous mobile robots are every day more common; they can be commercially available dotted with machine vision capabilities for diverse tasks and applications, like surveillance, 3D model reconstruction, localization and mapping based on stereo vision, cleaning, medical assistance, and assist handicapped and elderly people. All these robots missions require to the ability to work interactively in human environments and with online learning. Mobile robots with machine vision can be set up to detect, track, and avoid obstacles for optimal navigation. They can also estimate its pose and construct a 3D structure of a scene. Their vision can be based on stand-alone sensors or cameras based on sensors, filters, lens, and electronic and mechanical focus. Everyday cameras are more considered in research projects because they are affordable, inexpensive, robust, and compact. They capture a large amount of data reflecting both the photometric and geometric properties of the observed scene; however, they require considerable computing power and have a number of limitations related to the used sensors and their whole optical path design.

In this sense, *Machine Vision and Navigation* is important to modern science and industrial practical implementation. Hence, it is necessary to create new algorithms and systems to improve their performance. Although machine vision, control systems, and navigation applications for research and industrial areas are the primary interest in exploration, contaminated areas after natural and man-made disasters on our planet, as well as of unknown terrains on other planets, are also important, and the conjunctional use of these technologies and automatic systems is desirable.

The chapters in this book relate to contributions in machine vision applications. Each book chapter shows the state of the art in stand-alone sensors, cameras, methods, and 3D and 2D technologies in machine vision as well as the novel strategies in navigation performance.

These contributions are focused on optoelectronic sensors, 3D and 2D machine vision technologies, robot navigation, control schemes, motion controllers, intelligent algorithms, and vision systems, particularly on applications of unmanned aerial vehicle, autonomous and mobile robots, industrial inspection applications, and structural health monitoring. Recent advanced research in measurement and others areas where 3D and 2D machine vision and machine control play an important role as well as significant surveys and reviews about machine vision applications.

This book covers both theories and application of machine vision and navigation topics. In our opinion, this book should be attractive for potential consumers/citers because in our vision it is a well-balanced source of novel technologies in the area of machine vision and navigation with an explicit overview of recently existing systems, giving the comparative analysis of its features, advantages, and disadvantages. The topics are of interest to readers from a diverse audience in different areas of specialty as electrical, electronics, and computer engineering, technologists, and nonspecialist readers. The book is intended to be used as a text and reference work on advanced topics in machine vision and navigation. It is dedicated to academics, researchers, advanced-level students, and technology developers who will find this text useful in furthering their research exposure to pertinent topics in *Machine Vision and Navigation* and assisting in their future own research efforts in this field.

An Overview of Machine Vision and Navigation

The combination of machine vision and navigation is most promising nowadays, in recent years, we are finally seeing the full-scale release of daily-use devices, such as robot cleaners, robot assistants for the elderly, and so on. From previous experience, this is the best marker of the upcoming boom of demand of novel competitive technologies in the field. Covering all the topics of study in this book would be impossible; however, the most significant have been selected. The book contains 26 chapters which have been classified into five parts: (1) Image and Signal Sensors; (2) Detection, Tracking, and Stereoscopic Vision Systems; (3) Pose Estimation, Avoidance of Objects, Control, and Data Exchange for Navigation; (4) Aerial Imagery Processing; and (5) Machine Vision for Scientific, Industrial, and Civil Applications. These are briefly described in the following.

Chapter 1 is dedicated to image sensors and signal sensors used in current machine vision systems. Some of them suffer from low dynamic range and poor color constancy and are brittle and unmalleable, limiting their use in applications for which there will be considerable demand in the future. Most approaches aiming to resolve these inadequacies focus on developing improvements in the lighting, and software (processing algorithms) or hardware surrounding the photosensor such as filters is presented. Also discussed are other strategies that involve changing the architecture of the image sensor and the photo-sensing material; both have experienced recent success. Although they are yet to break fully into the market, image sensors developed from alternative solution-processed materials such as organic semiconductors and organohalide perovskites have immense potential to address the above issues and to "disrupt" machine vision technology.

Chapter 2 proposes a novelty passive vision sensor with a 360° horizontal field of view for mobile robots. With the implementation of this sensor, the robots can be provided with the ability of rapid detection of objects with a peripheral and central vision. The development of this sensor has been inspired by the peripheral/foveal typical vision in cooperation with the visual perception of vertebrates. It is based on the exploit of a catadioptric camera, while a rotating perspective camera makes it possible to measure distances, focusing attention on an already detected object, with a simple calibration methodology of the hybrid field-of-view vision systems. The sensor has been set up as a stand-alone and real-time sensor. It is a self-contained unit hosted in a single-board embedded computer with parallel processing capabilities that can be installed on any mobile robot, even those that have very limited computing power.

Chapter 3 focuses on the color and depth sensing technologies and analyzes how they play an important role in localization and navigation in unstructured environments. It discusses the important role of scanning technologies in the development of trusted autonomous systems for robotic and machine vision with an outlook for areas that need further research and development. A review of sensor technologies for specific environments is included, with special focus on the selection of a particular scanning technology to deal with constrained (indoor) or unconstrained (outdoor) environments. Fundamentals, advantages, and limitations of color and depth (RGB-D) technologies such as stereo vision, time of flight, and structured light and shape from shadow are discussed in detail. Strategies to deal with lighting, color constancy, occlusions, scattering, haze, and multiple reflections are evaluated in detail. It also introduces the latest developments in this area by discussing the potential of emerging technologies, such as dynamic vision and focus-induced photoluminescence.

Chapter 4 is a work developed for the construction of mixed image processor (IP) and neural networks (NNs) and image intensity transformation and the fundamentals of continuous logic cell (CLC) design based on current mirrors (CM) with functions of preliminary analog processing. The intention of the authors is to create video sensors and processors for parallel (simultaneous by pixel) image processing with advanced functionality and multichannel picture outputs to work in particular in hardware with high-performance architectures of neural networks, convolutional neural structures, parallel matrix-matrix multipliers, and special-processor systems. The theoretical foundations are analyzed. The mathematical apparatus of the matrix and continuous logic, their basic operations, and their functional completeness are described. The evaluation of their advantages and prospects for application in the design of biologically inspired devices and systems for processing and analysis of array signals are presented. It is demonstrated that some functions of continuous logic, including operations of normalized equivalence of vector and matrix signals, and the operation of a limited difference in continuous logic are a powerful basis for designing improved smart micro-cells for analog transformations and analog-digital encodings.

Chapter 5 proposes the use of a robotic total station assisted with cameras for detection and tracking of targets that are not signalized by reflectors. It introduces the principles of standard total stations, defining them as "modern geodetic multi-sensor systems measuring horizontal and vertical angles as well as distances using time-of-flight methods, thus delivering 3D-coordinates for static as well as moving objects." However, it focuses on the equipment of these systems with cameras and the application of photogrammetric techniques for the development of robotic image-assisted total stations for static and kinematic objects. Some examples of applications are described and a quality control study result is presented.

Chapter 6 offers a clear presentation of the methods and mathematical models for coordinate estimation using radar technologies and problems related to the recognition of object characteristics (landmarks) for mobile autonomous robots. Basically, it is devoted to the actual problem of navigating mobile autonomous robots on unknown terrains in the absence of GPS. Such a problem is considered solved if the robot is capable to detect a landmark and estimate own coordinates relative to the landmark. A reliable method for solving the problem is the simultaneous use of several measuring systems operating on different physical principles. In classical radar, the reliable detection of the echo signals from immovable landmark, which differ little from the echo signals that are reflected from the surrounding area, is impossible. Comparison of such signals is carried out in the chapter for various terrains at different lengths of electromagnetic waves. It is found that the only difference between them is the possible amplitude jump of signal, reflected from the landmark. This jump occurs during the movement of the robot or scanning the space by the robot antenna. The probability of detecting such a jump, the accuracy of the amplitude estimation, and the speed of the device operation are analyzed in the chapter based on the developed system of stochastic differential equations.

Chapter 7 overviews different machine vision systems in agricultural applications. Several different applications are presented but a machine vision system which estimates fruit yield, an example of an orchard management application, is discussed at length. From the farmer's perspective, an early yield prediction serves as an early revenue estimate. From this prediction, resources, such as employees and storage space, can more efficiently be allocated, and future seasons can be better planned. The yield estimate is accomplished using a camera with a color filter that isolates the blossoms on a tree when the tree is in its full blossom. The blossoms in the resulting image can be counted and the yield estimated. An estimate during the blossom period, as compared to when the fruit has begun to mature, provides a crop yield prediction several months in advance. Discussed as well, in this chapter, is a machine vision system which navigates a robot through orchard rows. This system can be used in conjunction with the yield estimation system, but it has additional applications such as incorporating a water or pesticide system, which can treat the trees as it passes by. To be effective, this type of system must consider the operating scene as it can limit or constrain the system effectiveness. Such systems tend to be unique to the operating environment.

Chapter 8 presents a deep review of stereoscopic vision systems (SVS), and their description, classification (geometric configuration, quantity of cameras, and other characteristics related with mathematical and computer processing), advantages, disadvantages, and applications in the current state of the art are stated. It is also noted that geometries of the SVS's shown in this chapter are ideal and are not considered factors that could affect the accuracy of measurements. The aim of the chapter is to provide information for everyone who wants to implement an SVS and needs an introduction to several available options to use the most convenient according to a specific application.

Chapter 9 is focused on the development of machine vision for robots, robot pose estimation, and 3D restructure of scenes through a set of matched correspondences and features extracted from multiple images. It provides modern and advanced strategies for image filtering and image feature extraction. It concentrates on stereo vision noise source that results in a 3D reconstruction of a scene. Strategies for image filtering and feature extraction are described based on techniques, such as Kalman Filter (KF), extended Kalman filter (EKF), and unscented Kalman filter (UKF). These filters are presented in order to increase the efficiency of visual simultaneous localization and mapping (VSLAM) algorithm to increase its efficiency. Practical examples in the field of robotics vision research are described, like pose tracking using UKF and stereo vision and localization approach-based 2D-landmarks map.

Chapter 10 is dedicated to the development of mathematical fundamentals for pose estimation. Pose estimation requires optimally estimating translation and rotation. The chapter is focused on rotation, since it involves nonlinear analysis. It is demonstrated how the computation can be done systematically if it is exploited the fact that the set of rotations forms a group of transformations, called the "special orthogonal group." A linear space spanned by infinitesimal rotations called the "Lie algebra" is defined. A computational procedure for minimizing the optimization function of a rotation based on Lie algebra formulation is described and applied to three computer vision problems: (1) Given two sets of 3D points, it is optimally estimated the translation and rotation between them in the presence of inhomogeneous anisotropic noise. (2) Given corresponding points between two images, it is optimally computed the fundamental matrix. (3) It is described the procedure of bundle adjustment for computing, from images of multiple points in the scene taken by multiple cameras, the 3D locations of all the points, and the postures of all the cameras as well as their internal parameters.

Chapter 11 shows a methodology for the accurate generation and tracking of closed trajectories over arbitrary, large surfaces of unknown geometry, using a robot whose control is based on the use of a non-calibrated vision system. The proposed technique referred to as camera-space manipulation is combined with a geodesic-mapping approach, with the purpose of generating and tracking a trajectory stored as a CAD model, over an arbitrarily curved surface, along with a user-defined position and orientation. A measure used to diminish the distortion caused by the mapping procedure and a technique for achieving closure of a given closed path, when this is tracked over large, non-developable surfaces, are presented herein. The performance of the proposed methodology was evaluated using an industrial robot with a large workspace whose geometry is not known in advance, combined with structured lighting used to reduce the complexity of the image analysis process.

Chapter 12 deals with generic image-based visual servoing control structure with onboard camera, based on the passivity theory and application. It gives a mathematical approach and a detailed literature research including also contributions of recent publications. The authors prove the convergence to zero of the control error and its robustness in the context of L_2-gain performance. A unified passivity-based visual servoing control structure considering a vision system mounted on the robot is presented. This controller is suitable to be applied for robotic arms, mobile robots, as well as mobile manipulators. The proposed control law makes the robot able to perform a moving target tracking in its workspace. Taking advantage of the passivity properties of the control system and considering exact knowledge of the target's velocity, the asymptotic convergence to zero of the control errors is proved. Later, it is carried a robustness analysis out based on L_2-gain performance, hence proving that control errors are ultimately bounded even when there exist bounded errors in the estimation of the target velocity. Both numerical simulation and experimental results illustrate the performance of the algorithm in a robotic manipulator, in a mobile robot, and also in a mobile manipulator.

Chapter 13 is about data exchange and task of navigation for robotic group. Robotic group collaboration in a densely cluttered terrain is one of the main problems in mobile robotics control. The chapter describes the basic set of tasks solved in model of robotic group behavior during the distributed search of an object (goal) with the parallel mapping. Navigation scheme uses the benefits of authors' original technical vision system (TVS) based on dynamic triangulation principles. According to the TVS output data were implemented fuzzy logic rules of resolution stabilization for improving the data exchange. The dynamic communication network model was modified and implemented the propagation of information with a feedback method for data exchange inside the robotic group. For forming the continuous and energy-saving trajectory, the authors are proposing to use two-step post-processing method of path planning with polygon approximation. Combination of our collective TVS scans fusion and modified dynamic data exchange network forming method with dovetailing of the known path planning methods can improve the robotic motion planning and navigation in unknown cluttered terrain.

Chapter 14 proposes a hierarchical navigation system combining the benefits of perception space local planning and allocentric global planning. Perception space permits computationally efficient 3D collision checking, enabling safe navigation in environments that do not meet the conditions assumed by traditional navigation systems based on planar laser scans. Contributions include approaches for scoring and collision checking trajectories in perception space. Benchmarking results show the advantages of perception space collision checking over popular alternatives in the context of real-time local planning. Simulated experiments with multiple robotic platforms in several environments demonstrate the importance of 3D collision checking and the utility of a mixed representation hierarchical navigation system.

Chapter 15 corresponds to a deep overview regarding autonomous mobile vehicles for wheeled ground applications. The different autonomy levels of vehicles are approached. The main concepts from path planning, going through the basic components that an autonomous vehicle must have, all the way to the perception it has of its environment, including the identification of obstacles, signs, and routes, are presented. The most commonly used hardware for the development of these vehicles is discussed. In the last part of this chapter, a case study, "Intelligent Transportation Scheme for Autonomous Vehicles in Smart Campus," is incorporated in order to help illustrate the goal of the chapter. Finally, an insight is included on how the innovation on business models can and will change the future of vehicles.

Chapter 16 is devoted to the approach of passive combined correlation-extreme systems implementing the survey-comparative method for recognition and analysis of images obtained from the machine vision system of a flying robot, which is able to significantly improve the correct localization of the objects in the image frame. A basic model for the radiometric channel operation of the correlation-extreme navigation systems is proposed. The factors that lead to distortions of the decisive function formed by the combined correlation-extreme navigation system of flying robots in a developed infrastructure are allocated. A solution of the problem of autonomous low-flying flying robots navigation in a developed infrastructure using the radiometric channel extreme correlation navigation systems (CENS), when the size of the solid angle of associated object is much larger than the size of the partial antenna directivity diagram (ADD), is proposed.

Chapter 17 is focused in the description of an analytic image stabilization approach where pixel information from the focal plane of the camera is stabilized and georegistered in a global reference frame. The aerial video is stabilized to maintain a fixed relative displacement between the moving platform and the scene. The development of the algorithm that is able to stabilize aerial images using its available weak/noisy GPS and IMU measurements, based on the use of analytically defined homographies between images and minimizing the cost function on a 2D equation space, is presented. The algorithm is applied in the Defense Advanced Research Projects Agency (DARPA) video and image retrieval and analysis tool (VIRAT) data set and wide area motion images (WAMI).

Chapter 18 describes a visual servo controller designed for an unmanned aerial vehicle dedicated to tracking vegetable paths. In the inspection and data collection of large areas as crop fields, where an aerial vehicle should follow an object's line accurately, autonomous flight is a desirable feature with unmanned aerial vehicles. To attain this objective, three visual servo controllers are proposed; one of them is position based and the other two are image based using inverse Jacobian and concepts of passivity, respectively. All controllers are developed based on the kinematic model of the vehicle, and a dynamic compensation is designed to be added in cascade with the kinematic one. The performance of the control systems is compared through simulation results. The main contribution is the development of the image-based controller using passivity properties of the system, the stability and robustness analysis, and the comparative performance with other controllers when used for an unmanned aerial vehicle following vegetal lines. These comparative results are valuable to choose the appropriate driver for a specific application.

Chapter 19 is the result of a deep study and research of multimedia compression advances, focusing on the use of the integer discrete cosine transform, the wavelet transform, and fovea centralis. Data compression is concerned with minimization of the number of information-carrying units used to represent a given data set. Such smaller representation can be achieved by applying coding algorithms. Coding algorithms can be either lossless algorithms that reconstruct the original data set perfectly or lossy algorithms that reconstruct a close representation of the original data set. Both methods can be used together to achieve higher compression ratios. Lossless compression methods can either exploit statistical structure of the data or compress the data by building a dictionary that uses fewer symbols for each string that appears on the data set. Lossy compression on the other hand uses a mathematical transform that projects the current data set onto the frequency domain. The coefficients obtained from the transform are quantized and stored. The quantized coefficients require less space to be stored.

Chapter 20 shows a method to solve the stairway localization and recognition problem for both indoor and outdoor cases by using a convolutional neural network technique. This work has been motivated because for blind and visually impaired persons, this assistive technology application has an important impact in their daily life. The proposed algorithm should be able to solve the problem of stair classification for indoor and outdoor scenes. The proposed idea describes the strategy for introducing an affordable method that can recognize stairways without taking into account the environments. Firstly, this method uses stair features to classify images by using convolutional neural networks. Secondly, stairway candidate is extracted by using the Gabor filter, a linear filter. Thirdly, the set of lines belonging to the ground plane are removed by using the behavioral distance measurement between two consecutive frames. Finally, it is extracted from this step the tread depth and the riser height of the stairways.

Chapter 21 gives a deep review of new- and advanced-phase triangulation methods for 3D-shape measurements in scientific and industrial applications. The mathematical methods for phase triangulation are presented, which allow the measurement of 3D data under the conditions of arbitrary light-scattering properties of the scanning surface, varying measurement setting external illumination and limited depth of field of optical elements of the source and receiver of optical radiation. The book chapter provides a deep mathematical approach about the proposed steady-state method for decoding phase images and presents a method for nonlinearity compensation of the source-receiver path of optical radiation in 3D measurements. The application of the proposed methods provides higher metrological characteristics of measuring systems and expands the functionality and the range of application of optical-electronic systems for geometric control in the production environment.

Chapter 22 presents a thermal image processing method to monitor a moving melt pool of a blown powder deposition process using infrared thermography. Thereby, the moving melt pool is created on a substrate material by the use of a laser and a motorized work table, where the material is (stainless steel 316) deposited in a layer-by-layer sequence on the substrate material. The steel is placed in powder form on the substrate and brought to its melting point by means of a 1 kW fiber laser with a wavelength of 1064 nm. By controlling a fixed melting pot size in closed-loop configuration, a consistent material deposition and layer thickness of the deposited material are ensured. For the feedback of the closed-loop control, an energy management system and a height control system are used to track the total spectral radiance of the melt pool and to track the top of the deposited material. The chapter gives a good and practical overview of the blown powder deposition process using infrared thermography and names the used technologies to implement the melting and tracking process. It uses Planck's law to define the spectral radiance of the melt pool for the energy management system. It also presents infrared thermographs to detect different temperature regions of the melt pool.

Chapter 23 describes the importances of image processing of measurement signals that are contaminated with noise for accurate fault detection and isolation in machines. This chapter presents processing filters to detect step changes in noisy diagnostic signals of a gas turbine, which the authors use as indicator for an onset of a single fault of these signals. By using the process filters, the noise of the gas turbine diagnostic signals is reduced and then examined for a step change. Various linear and nonlinear process filters are described and compared, where the weighted recursive median (WRM) filter is highlighted for good noise reduction. Also, the ant colony optimization (ACO) method is used to calculate the integer weights of the weighted recursive median filter.

Chapter 24 proposes a new method to control and automatize the position of three-axis piezoelectric nano-manipulators that handle a GSG nanoprobing to ensure the precise positioning of the probe on the substrate under test. The method is based on a measurement setup that consists of a vector network analyzer (VNA) connected through coaxial cables to miniaturized homemade coplanar waveguide (CPW) probes (one signal contact and two ground contacts), which are themselves mounted on three-axis piezoelectric nano-manipulators SmarActTM. The device under test (DUT) is positioned on a sample holder equipped also with nano-positioners and a rotation system with μ-degree resolution. The visualization is carried out by a scanning electron microscope (SEM) instead of conventional optics commonly found in usual on-wafer probe stations. This study addresses the challenge related to the control of nano-manipulators in order to ensure precisely the contact between the probe tips and the DUT to be characterized.

Chapter 25 shows the design of an industrial inspection system for plastic parts. The development of user-friendly design and training tool for convolutional neural networks (CNNs) and support vector machines (SVMs) as an application development environment based on MATLAB is presented. As the first test trial, an application of deep CNN (DCNN) for anomaly detection is developed and trained using a large number of images to distinguish undesirable small defects such as crack, burr, protrusion, chipping, spot, and fracture phenomena that occur in the production process of resin molded articles. Then, as the second test trial, a SVM incorporated with the AlexNet and another SVM incorporated with our original sssNet are, respectively, designed and trained to classify sample images into accepting as OK or rejecting as NG categories with high categorization rate. In the case of these SVMs, the training can be conducted by using only images of OK category. The AlexNet and the sssNet are different types of DCNNs, whose compressed feature vectors have 4096 and 32 elements, respectively. The two lengths of compressed feature vectors are used as the inputs for the two types of SVMs, respectively. The usability and operability of the developed design and training tool for DCNNs and SVMs are demonstrated and evaluated through training and classification experiments.

Chapter 26 is dedicated to a structural health monitoring application. It describes that due to the increase of frequency and weight of commercial ship trips in waterways, bridges are more vulnerable than ever to ship-bridge collision accidents. It explains that there are plenty of reports of such cases all over the world, leading to millions of economic losses. For ancient bridges, irreparable damage might come in the sense of cultural value except for economic losses. The development of computer vision-based technology provides an active defense method to prevent the damage in advance. This chapter presents a computer vision-based method for ship-bridge collision assessment and warning for an ancient arch bridge over the Beijing-Hangzhou Grand Canal in Hangzhou, China. The structural characteristic and current status of the arch bridge were analyzed. The traffic volume and parameters of passing ships including velocity and weight were investigated. Water area in both sides of the bridge was divided into three different security districts corresponding to different warning levels. Image processing techniques were exploited to identify the types of ships for tracking. The potential of ship-bridge collision was assessed, and warning was generated according to the security evaluation.

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Abbreviations

2D	Two-dimensional
3D	Three-dimensional
4WDDMR	Four-wheeled differential drive mobile robot
AAM	Auto-associative memory
AB	Aborted
ABAC	Adaptive binary arithmetic coding
ABC	Analog-digital basic cell
ACO	Ant colony optimization
ACS	Automated control systems (Meaning in Chap. 16)
ACS	Ant colony system (Meaning in Chap. 23)
AD_*	Anytime D_*
ADC	Analog to digital converter
ADD	Antenna directivity diagram
AFV-SPECK	Adaptive fovea centralis set partitioned embedded block codec
AlexNet	A well-known convolutional neural network designed by Alex Krizhevsky
AM	Associative memory (Meaning in Chap. 4)
AM	Additive manufacturing (Meaning in Chap. 22)
AMCW	Amplitude modulated continuous wave
AO	Absolute orientation
AP	Antenna pattern
APD	Avalanche photo diode
API	Application programming interface
AS/RS	Automated storage and retrieval system
ASCII	American standard code for information interchange
ASIC	Application-specific integrated circuit
AVC	Advance video coding
AWFV-Codec	Adaptive wavelet/fovea centralis-based codec
BA	Bundle adjustment
BC	Basic cell (Meaning in Chap. 4)

BC	Bumper collision (Meaning in Chap. 14)
BDS	BeiDou navigation satellite system
Bel	Degree of belief
BGR	Blue green red color space
BIA	Binary image algebra
BLS	Bottommost line segments
BM	Block matching
BP	Back propagation algorithm
BPD	Blown powder deposition
bpp	Bits per pixel
CAD	Computer-aided design
CAF	Correlation analysis field
Caffe	Convolutional architecture for fast feature embedding
CAS	Computer-assisted surgery
CCC	Coefficient of cross correlation
CCCA	Current-controlled current amplifiers on current mirror multipliers
CCD	Charge-coupled device
CDF9/7	Cohen-Daubechies-Feauveau wavelet
CDNE	Complementary double NE
CENS	Channel extreme correlation navigation systems
CENS – I	CENS in which information is currently removed at a point
CENS – II	CENS in which information is currently removed from a line
CENS– III	CENS in which information is currently removed from an area (frame)
CFA	Color filter array
CI	Current image
CIF	Common intermediate format
CIS	Cmos image sensors
CL	Continuous logic
CLC	Continuous logic cell
CLEM	Continuous logical equivalence model
CLF	Continuous logic function
CM	Current mirror
CML	Concurrent mapping and localization
CMM	Current multiplier mirror
CMOS	Complementary metal-oxide semiconductor
CMYK	Cyan, magenta, yellow, black color space
CNC	Computer numerical control
CNN	Convolutional neural network
CNN-CRF	Convolutional neural network-conditional random field
Cov	Covariance
CPR	Cycles per revolution
CPU	Central processing unit
CPW	Coplanar waveguide
CQDs	Colloidal quantum dots

CS	Control systems
CSM	Camera-space manipulation
C-Space	Configuration space
CUDA	Compute unified device architecture
CVM	Curvature velocity method
CWT	Continuous wavelet transform
D_*	Specific detectivity (Meaning in Chap. 1)
D_*	Dynamic a_* (Meaning in Chap. 14)
D/A	Donor-acceptor
DAC	Digital-to-analog converter
dB	Decibel
DBSCAN	Density-based spatial clustering of applications with noise
DC	Digital-analog cell
DCF	Decision function
DCT	Discrete cosine transform
DF	Decision function
DGPS	Differential global positioning system
DL	Deep learning
DLP	Dwa local planner
DOEP	Digital optoelectronic processor
DOF	Degree of freedom
DoG	Difference of gradient
DSSC	Dye-sensitized solar cells
DUT	Device under test
DWA	Dynamic window approach
DWT	Discrete wavelet transform
EB	Elastic bands
ECS	Environment cooling system
EDM	Electronic distance measurement
EGT	Exhaust gas temperature
EKF	Extended Kalman filter
EM	Equivalence model
EMR	Electromagnetic radiation
EMW	Electromagnetic waves
EO	Exterior orientation
EQ_CL	Equivalent continuous-logical
EQE	External quantum efficiency
ExG-ExR	Excess green minus excess red vegetation index
FCL	Flexible collision library
FDI	Fault detection and isolation
FET	Field-effect transistor
FIP	Focus-induced photoluminescence
FIR	Finite impulse response
FIT	Frame interline transfer
FMCW	Frequency-modulated continuous wave

FNS	Fundamental numerical scheme
FO	False object
FoV	Field of vision
FPGA	Field programmable gate array
FPS	Frames per second
FR	Flying robots
FT	Frame transfer
FVHT	Fovea centralis hierarchical trees
FW	Fixed window
FWHM	Full width at half maximum
FWT	Fast wavelet transform
FW-UAV	Fixed wings unmanned aerial vehicle
G	Gray
GaN nanowires	Gallium nitride nanowires
GIF	Graphics interchange format
GNSS	Global navigation satellite system
GPGPU	General purpose graphics processing unit
GPS	Global positioning system
GPU	Graphics processing unit
GRV	Gaussian random variable
GSD	Ground sampling distance
GSG	Ground signal ground
GVD	Generalized voronoi diagram
HAM	Hetero-associative memory
HD	High definition
HEVC	High efficiency video coding
HF	High frequency
HH	Horizontal histogram
HIL	Hardware-in-the-loop
HPC	High pressure compressor
HPT	High pressure turbine
HSV	Hue-saturation-value (color model)
HVS	Human visual system
Hz	Horizontal
IATS	Image-assisted total station
ICP	Integrated color pixel
ID	Identification
iDCT	Integer discrete cosine transform
IDE	Integrated development environment
IEEE	Institute of electrical and electronics engineers
IF	Informational field
IIR	Infinite impulse response
iLWT	Inverse LWT
IMU	Inertial measurement units
INS	Inertial navigation system

IO	Interior orientation
IoT	Internet of things
IP	Image processor
IPT	Image process technology
IR	Infrared
IRNSS	Indian regional navigation satellite system
iSPECK	Inverse SPECK
IT	Information technologies
IT SB RAS	Institute of Thermophysics Siberian branch of Russian academy of Science
JBIG	Joint bi-level image group
J_{d}	Dark current
JPEG	Joint photographic experts group
JPEG2000	Joint photographic experts group 2000
J_{ph}	Photocurrent
JSR	Just solidified region
k-d tree	k-dimensional tree
KF	Standard Kalman filter
K_{I}	Integral gain
K-nn	K-nearest neighbors
K_{P}	Proportional gain
ILSVRC2012	Large-scale visual recognition challenge 2012
LCL	Lossless compression limit
LCM	Lane curvature method
LDR	Linear dynamic range
LED	Light-emitting diode
LIDAR	Light detection and ranging
LIP	List of insignificant pixels
LIS	List of insignificant sets
LoG	Laplacian of Gaussian
LPC	Low-pressure compressor
LPF	Low-pass filter
LPT	High-pressure compressor
LSP	List of significant pixels
LWT	Lifting wavelet transform
MAAM	Multi-port AAM
MAD	Mean of Absolute Differences
MAE	Mean absolute error
MAP	Maximize the Posterior estimation
MAR	Mobile autonomous robots
MATLAB	A high performance computing environment provided by MathWorks
MAV	Micro aerial vehicle
MDPG	Maximum distance of plane ground
MEMS	Microelectromechanical systems

MEO	Medium earth orbit
MHAM	Multi-port hetero-associative memory
MIMO	Multi input and multi output
MIPI	Mobile industry processor interface
MIS	Minimally invasive surgery
MIT	Massachusetts Institute of Technology
MLA	Array of microlenses
MLE	Maximum likelihood estimator
MPEG	Moving picture experts group
MPixel	Mega pixel
MRS	Multi-robot systems
MSCA	M-estimator Sample Consensus
MSE	Mean squared error
MUTCD	Manual on uniform traffic control devices
MVS	Machine vision systems
N1	High rotor speed
N2	Low rotor speed
NCC	Normalized cross correlation
ND	Nearness diagram
NE	Neural element
NEP	Noise equivalent power
Neq	Normalized equivalence
Neqs	Neuron-equivalentors
NEU	North-east-up
NIR	Near infrared
NN	Neural network
NnEq	Normalized nonequivalence
NS	Navigation system
NSEqF	Normalized spatial equivalence function
PA	Candidate area
PE	Number of areas
PL	Number of line
PP	Number of pixels
OB	Object of binding
OC	Opposite cathetus
OD	Obstacle detection
OE-VLSI	Optoelectronic very large-scale integration
OFET	Organic field-effect transistor
OHP	Organohalide perovskite
OLED	Organic light-emitting diode
OPD	Organic photodiode
OPT	Organic phototransistor
OR	Object of binding
ORB	Oriented FAST and Rotated BRIEF
OSC	Organic semiconductor

PC	Personal computer
PCL	Point cloud library
PCX	Personal computer exchange
pdf	Probability density function
PI	Proportional-plus-integral
PID controller	Proportional-integral-derivative controller
PiPS	Planning in perception space
pixel	Picture element
PL	Positioning laser
PM	Propagation medium
PNG	Portable network graphics
ppi	Pixels per inch
PPR	Pulses per revolution
PRM	Probabilistic road map
PSNR	Peak signal-to-noise ratio
PT	Phototransistor
QR	Code-quick response matrix code
RADAR	Radio detection and ranging
RANSAC	Random sample consensus
RAR	Roshal archive file format
RCS	Radar cross section
ReLU	A rectified linear unit function
RF	Radio frequency
RFBR	Russian fund of basic research
RGB	Red, green, blue
RGB-D	Red, green, blue depth
RI	Reference image
RLE	Run length encoding
RM	Radiometric (Meaning in Chap. 16)
RM	Recursive median (Meaning in Chap. 23)
RMI	Radiometric imaging
RMS	Root mean square
RMSE	Root mean square error
RO	Relative orientation
ROI	Region of interest
ROIC	Read-out integrated circuitry
ROS	Robot operating system
ROV	Remotely operated vehicle
RRT	Rapidly exploring random tree
RTS	Robotic total station
RW-UAV	Rotary wings unmanned aerial vehicle
S/R	Storage and retrieval
SA	Scanning aperture
SAD	Sum of absolute differences
SAE	Society of automotive engineers

SD	Standard deviation
SD_NEF	Spatially dependent normalized equivalence function
SDPN	Sensors of different physical nature
SE(2)	Special Euclidean group for two-dimensional space
SE(3)	Special Euclidean group for three-dimensional space
SEM	Scanning electron microscope
SfM	Structure from motion
SGBM	Semi-global block matching
SHD	Sample and hold device
SHM	Structural health monitoring
SI	Source image
SI EM AM	Spatially invariant equivalence model associative memory
SIFT	Scale invariant feature transform
SLAM	Simultaneous localization and mapping
SLECNS	Self-learning equivalent-convolutional neural structure
SM	Simple median
SMC_ADC	Multi-channel sensory analog-to-digital converter
SMO	Sequential minimal optimization algorithm
SoC	System on a chip
SPAD	Single-photon avalanche diodes
SPECK	Set partitioned embedded block codec
SPIHT	Set partitioning in hierarchical tree
sRGB	Standard Red, Green, Blue color space
SS	Sighting surface
SSD	Sum of squared differences
SSIM	Structural similarity index
STP	Spanning tree protocol
SURF	Speeded-up robust feature
SVD	Singular value decomposition
SVM	Support vector machine
SWNT	Single walled nanotube
TC	Transfer characteristics
TCC	Turbine cooling casing
TCP/IP	Transmission control protocol/Internet protocol
TEB	Timed elastic bands
TensorFlow	An open source software library which can be used for the development of machine learning software such as neural networks
TFD	Transverse field detector
TFLOPS	Tera floating point operations per second
TLS	Total least squares algorithm
TM	Trademark
TNM	Technical navigation means
TO	Time-out
ToF	Time of flight
TPCA	Time-pulse-coded architecture

TSR	Traffic sign recognition
TVS	Technical vision system
UABC	Universidad Autonoma de Baja California
UAV	Unmanned aerial vehicle
UGV	Unmanned ground vehicle
UKF	Unscented Kalman filter
UL	Unit load
ULE	Universal (multifunctional) logical element
USB	Universal serial bus
V	Vertical
vAOV	Vertical angle of view
Var	Variance
VFH	Vector field histogram
VH	Vertical histogram
VIRAT	DARPA video and image retrieval and analysis tool
VMO	Vector or matrix organization
VNA	Vector network analyzer
VO	Visual odometry
VPH	Vector polar histogram
VSLAM	Visual simultaneous localization and mapping
WAAS	Wide area aerial surveillance
WAMI	Wide area motion imagery
WAPS	Wide-area persistent surveillance
WebP	Webp
WF	Fuel flow
WFOV	Wide field of view
WRM	Weighted recursive median
WT	Wavelet transform
$Y'C_BC_R$	Luma Chrominance color space
ZIP	.ZIP file format

Chapter 4
Design and Simulation of Array Cells of Mixed Sensor Processors for Intensity Transformation and Analog-Digital Coding in Machine Vision

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Acronyms

AAM	Auto-associative memory
ABC	Analog-digital basic cell
ADC	Analog–to-digital converter
AM	Associative memory
BC	Basic cell
BIA	Binary image algebra
CCCA	Current-controlled current amplifiers on current mirror multipliers
CDNE	Complementary double NE
CL	Continuous logic
CLC	Continuous logic cell
CLEM	Continuous logical equivalence model
CLF	Continuous logic function
CM	Current mirror
CMM	Current multiplier mirror
CMOS	Complementary metal-oxide-semiconductor
CNN	Convolutional neural network
DAC	Digital-to-analog converter
DC	Digital-analog cell
DOEP	Digital optoelectronic processor
EM	Equivalence model
EQ_CL	Equivalent continuous-logical
FPAA	Field-programmable analog array

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G	Gray
HAM	Hetero-associative memory
IP	Image processor
MAAM	Multi-port AAM
MHAM	Multi-port hetero-associative memory
MIMO	Multi-input and multi-output
MLA	Array of microlenses
NE	Neural element
NEq	Normalized equivalence
NEqs	Neuron equivalentors
NN	Neural network
NnEq	Normalized nonequivalence
NSEqF	Normalized spatial equivalence function
OE-VLSI	Optoelectronic very large scale integration
SD_NEF	Spatially dependent normalized equivalence function
SHD	Sample and hold device
SI EM AM	Spatially invariant equivalence model of associative memory
SLECNS	Self-learning equivalent convolutional neural structure
SMC_ADC	Multichannel sensory analog-to-digital converter
TC	Transfer characteristics
TPCA	Time-pulse-coded architecture
ULE	Universal (multifunctional) logical element
VMO	Vector or matrix organization

4.1 Introduction

To create biometric systems, computer vision systems are needed to solve the problem of recognizing objects in images. There are many known methods and means to address these problems [1, 2]. In most recognition algorithms, the most frequently used operation is the comparison of two different images of the same object or its fragments. The mutual 2D function of correlating a reference fragment with the current offset image fragment is also most often used as a discriminant measure of their mutual comparison. With a strong correlation of images in their set to improve the accuracy and probability, the quality of comparison of the noisy current fragment and the reference image, as shown in [3], it is desirable to use methods of comparison, image selection, based on measures of mutually equivalent two-dimensional spatial functions transformations and adaptive correlation weightings. Various models of neural networks (NN) are actively used as a tool for image recognition and clustering. The latter is also widely used for modeling pattern recognition, biometric identification, associative memory (AM), and control of robotic devices. In [4, 5], equivalence models (EM) of auto-associative memory (AAM) and hetero-associative memory (HAM) were proposed. The EMs have an increased memory capacity (3–4 times higher than the number of neurons) relative to the number of neurons (4096 and more) and the ability to compare, store, and retrieve to recognize strongly correlated and noisy images of large dimension, as was shown in [6–8]. These models allow you to recognize fragments (64×64 and more) with a significant percentage (up to 25–30%) of damaged pixels [5, 7, 9, 10]. Models of multi-port AAM (MAAM) and multi-port hetero-associative memory (MHAM) for associative image storage and recognition were investigated in [7, 8], the main idea of which was originally published in [4]. Mathematical models and AM implementations based on EMs were initiated in [4] and described in detail in papers [7–9], and their modifications in [11–13]. For analysis and recognition, the problem of clustering various objects must be solved. This previous clustering allows you to organize the correct automated grouping of the processed data, conduct cluster analysis, evaluate each cluster on the basis of a set of attributes, put a class label, and improve subsequent classification and recognition procedures. The significant advantages of the EM for creating MAAM and MHAM on their basis [8, 11, 12] and improved neural networks [5–9], made it possible to suggest new modifications of MHAM for parallel cluster image analysis [11, 12] and their hardware implementations on parallel structures, matrix-tensor multipliers, equivalentors with spatial and temporal integration [8, 9, 12–14]. Spatially non-invariant models and their implementation for image recognition and clustering were considered in [8, 12], and only in [1, 2, 9, 11], spatial-invariant image recognition models were considered, but not clustering. More generalized spatially invariant (SI) equivalence models (EMs) are invariant to spatial displacements and can be used for clustering images and their fragments, and therefore, the study of such models is an urgent task [14–17]. In addition, as our analysis shows, these models, described in our works [1–10] and known for more than 20 years, are very closely related to the operations of convolution of images. In the most promising paradigms of convolutional neural networks (CNN) with deep learning [18–24], the main operation is convolution. But they reveal that regularities on the basis of existing patterns or filters require complex computational procedures in their training. Jim Crutchfield of UC Davis and his team are exploring a new approach to machine learning based on pattern discovery. Scientists create algorithms to identify previously unknown structures in data, including those whose complexity exceeds human understanding. New possible ways of self-learning based on such advanced models were considered in [25]. It explained some important fundamental concepts, mechanisms of associative recognition and modeling processes of transformation and learning on the basis of understanding the principles of biological neural structures functioning. Patterns were identified in such models for binary slices of digitized multilevel images, and their implementations were proposed, and refer article [26] for multilevel images without prior binarization. But, as will be explained below, for all progressive models and concepts and nonlinear transformation of signals, image pixel intensities are necessary.

The bottleneck between the processor and the memory or processors is very slow interconnects. The increase in the integration density of devices further aggravates the problem, since more channels are required for communication outside the crystal. The use of optical interconnects is discussed as an alternative to solve the problems mentioned. The use of optics or optoelectronics for interconnects outside the crystal and inside the crystal was demonstrated in [27]. This problem in such OE-VLSI is solved by implementing external interconnects not with the edge of the chip, but with arrays of optical detectors and light emitters, which allow implementing the stack architecture of a three-dimensional chip [28]. But in this case, the combination of various passive optical elements with active optoelectronic and electronic circuits in one system is also an unsolved problem. Intelligent detector circuits can be thought of as a subset of OE-VLSI circuits. They consist only of arrays of photodetectors, which can be monolithically integrated with digital electronics in silicon and circuits for analog-digital conversion. This greatly simplifies the design of OE-VLSI circuits, which must additionally contain only light-emitting devices, and the latter can also be implemented in silicon [29]. Such intelligent detectors with a frame [30] show a large scope and market potential. In this regard, our approach also relies on an intelligent pixel-like structure combining parallel detection of signals with parallel processing of signals in a single circuit. To realize the fastest processing, each pixel has its own analog and analog-digital node. One of the important directions for solving various scientific problems is parallel processing of large arrays (1D or 2D) of data using non-traditional computational MIMO-systems and matrix logics (multi-valued, sign, fuzzy, continuous, neuro-fuzzy, etc.) and the corresponding mathematics [31–34]. For realizations of optical learning neural networks (NN) with a two-dimensional structure [31], continuous logical equivalence models (CLEM) NN [32–34] require elements of matrix logic as well as an adequate structure for vector matrix computing procedures. Advanced parallel computing structures and processors with time-pulse signal processing [35] require parallel processing and parallel inputs/outputs. The generalization of scalar two-valued logic on the matrix case led to the intensive development of binary image algebra (BIA) [36] and logical elements of a two-dimensional array for optical and optoelectronic processors [33, 35, 37–39]. One of the promising areas of research is the use of time-pulse-coded architectures (TPCA), which were considered in papers [40, 41], which, through the use of two-level optical signals, not only increase functionality (up to universality), increase noise immunity and stability, and reduce the requirements for alignment and optical system but also simplify the control circuit and settings for the required functions and keep intact the entire methodological basis of these universal elements regardless of the length of the code word and the type of logic. Mathematical and other theoretical foundations of universal (multifunctional) logical elements (ULE) of the matrix logical design with a fast programmable setting, where the unification of functional bases is expedient, and the need to use ADC arrays were considered in [42, 43]. An ADC is a continuous-discrete automation that performs the conversion of an analog value x by its interaction with standard sizes in a discrete output code. Aspects of the theory and practice of designing and using ADCs and

DACs are so broadly outlined that it is even difficult to choose the most general works. At the same time, in the last 20–30 years, optical methods and means for parallel digital image processing have been intensively investigated, which, unlike analog ones, have high accuracy and a number of significant advantages. Certain success has been achieved in the field of creating two-dimensional matrix logic devices, storing image-type data for such parallel information systems and digital optoelectronic processors (DOEP) [38] with a performance of 10^{12}–10^{14} bits per second. Most vector-matrix and matrix-matrix multipliers [39] use 1D linear and 2D matrix multichannel ADC [43–45]. A bottleneck in parallel DOEP is an ADC, which, unlike traditional input systems with scanning or sequential parallel reading and output, must in parallel fully perform ADC conversion of a large number of signals (256×256 pixels or more) and provide an input speed of up to 10^6–10^7 frames per second. Therefore, there is a need of multichannel ADC with several parallel inputs and outputs, with vector or matrix organization (VMO) [43–45], and the channels operate in parallel and provide low power consumption, simple circuit implementation, short transformation time, low input level, acceptable word length, etc. In addition, such a VMO ADC can also perform other functions, for example, the computation of logical matrix operations, digital filtering, and digital addition-subtraction of images. For multichannel multisensor measuring systems, especially for wireless ones, ADCs with very low consumption and high accuracy and speed are required. In papers [46–52] design of ADCs, current comparators, and their applications were considered. But these comparators are very high speed, consist of many transistors, and have high consumption power. Equivalent (EQ) continuous-logical (CL) ADC, which was considered in [43–45, 51], provided high performance with a smaller amount of equipment since it consisted of n-series-connected analog-digital basic cells (ABC). Such cells implement CL-functions on CMOS-transistors operating in the current mode. The parameters and performance of such CL ADCs, including the type of output codes, are influenced by the selection of the required continuous logic functions for the analog-digital conversion and the corresponding ABC scheme. The simplicity of these CL ADCs makes it possible to realize a significant number of multichannel converters for optical parallel and multisensor systems. The proposed CL ADC schemes are more preferable specifically for such applications where parallelism and large size arrays are required. Based on the above, the purpose of our chapter is to design and simulate various variants of the technical implementation of continuously logical basic cells (CL BC) based on current mirrors (CM) and multichannel sensory analog-to-digital converters (SMC ADC) with the functions of preliminary analog and subsequent analog digital processing for image processors (IP) and sensor systems. In addition, in our previous works, the accuracy characteristics of the ADC were not considered, and no estimates of conversion errors were made for different possible modes and modifications of such basic cells and ADCs as a whole. That is why the purpose of the present work is also to evaluate ADC errors, demonstrate them by specific experimental results, and also further enhancements of such ADCs and their basic cells, which significantly expand their functionality and the range of problems they solve.

4.2 Simulation of Array Cells for Image Intensity Transformations and Theoretical Mathematical Background

4.2.1 Substantiation of the Need to Design Devices for Parallel Nonlinear Image Intensity Transformations in Self-Learning Equivalent Convolutional Neural Structures (SLECNS)

For neural networks and associative memory systems, generalized equivalence models using the functions of nonlinear normalized equivalences of matrices and tensors were developed. They use spatially dependent normalized equivalence functions (SD_NEF) [6], which are defined as:

$$\tilde{\mathbf{e}}(A, B) = \frac{A \tilde{*} B}{I \times J} = \frac{1}{I \times J} \sum_{i=1}^{I} \sum_{j=1}^{J} \left(a_{\varsigma+i,\eta+j} \sim b_{i,j}\right) \tag{4.1}$$

where $\tilde{\mathbf{e}} = \left[e_{\varsigma,\eta}\right] \in [0, 1]^{(N-I+1)\times(M-J+1)}$ and symbol $(\tilde{*})$ indicate a spatial convolution, but with an element-wise operation of not multiplication, but "equivalence." In accordance with the principle "the strongest survives" and the strengthening of the nonlinear action of the components, depending on the level of their values, the elements of the matrix $\tilde{e}(\tilde{e})$ and of other intermediate SD_NEF are transformed using of auto-equivalence operations [13] with different parameters p_1, p_2. The higher the parameters p_1, p_2 in p-step auto-equivalence, that is, the more "competing" nonlinear transformations, the faster the process of recognition and state stabilization, as studies show with the help of energy equivalent functions [6, 26, 53]. The number of iterations necessary for successful recognition depends on the model parameters and, as experiments show, is significantly smaller compared to other models and does not exceed just a few. Changing the parameters p_1, p_2 it is possible to obtain all the previously known EMs [5–13]. To implement the proposed new subclass of associative neural systems, certain new or modified known devices are needed that can calculate the normalized spatial equivalence functions (NSEqFs) with the necessary speed and performance [1, 6, 10]. We called such specialized devices the image equivalentors [4, 6, 9, 10, 13], which are, in essence, a doubled correlator [54] or a doubled convolver. For the input image S_{inp}, learning array matrix **A**, which is a set of reference images, the general SI EM AM is proposed [11, 14, 15] and modeled, where after the first and the second steps of the algorithm, the element-wise equivalence convolution and nonlinear transformations were calculated. Research results of the generalized SI EM AM confirmed advantages and improved characteristics and the possibility to recognize with interferences up to 20–30% [14, 15]. Works [12, 14] described a clustering method based on the simultaneous calculation of the corresponding distances between all cluster neurons and all training vectors using such MAAM and MHAM. As metrics, we use generalized nonlinear normalized vector equivalence functions, which gives good convergence and high speed of models, see papers [12, 14–17]. An iterative learning process that uses a learning matrix and consists of calculating the optimal set of weight vectors for all cluster neurons is described by the proposed model. Optimal patterns are formed by such an iterative procedure, based on the search for patterns and tangible fragments of objects that are in the set of trained images. Patterns of recognition and clustering of images that combine the learning process with the process of recognition are proposed in [25, 26]. For our EMs and all known convolutional neural networks, it is necessary to determine the convolutions of a large number of patterns from the set of standards with the current image fragment in each layer in the learning process. Large images require a large number of filters for image processing, as studies show, and the size of filters, as a rule, is also large. Therefore, the acute problem is to significantly improve the computational performance of such CNN. Therefore, the last decade was marked by the activation of work aimed at creating specialized neural accelerators, which calculate the comparison function of 2 two-dimensional arrays and use the multiplication and addition accumulation operations. Unlike most papers, in our works, we use those functions of normalized equivalence in which there is no multiplication operation. But, as our studies show, equivalent models also allow us to construct convolutional equivalence structures and self-learning systems. Therefore, using our approaches to the construction of a one-dimensional neuron equivalentor [55–58], we considered the structure of a two-dimensional neuron equivalentor, generalized for processing two-dimensional arrays. The block diagram of the main unit of self-learning equivalent convolutional neural structures (SLECNS) [26] is shown in Fig. 4.1a. The required number of convolutions $e_0 - e_{n-1}$, depending on the number of filter templates $\mathbf{W}_0 - \mathbf{W}_{n-1}$, is formed from the matrix $\mathbf{X}$. Convolutions are represented by matrices with multilevel values, unlike binary ones, which we used earlier. Each filter is compared with the current fragment of the matrix, and equivalent measures of proximity or other measures, such as a histogram, are used as a measure of the similarity of the fragment of the matrix $\mathbf{X}$ and the filter. Therefore, interpretation method for spatially invariant case requires the calculation of spatial features convolution-type $\mathbf{E}^m = \mathbf{W}^m \overset{t}{\tilde{\otimes}} \mathbf{X}$, where $E^m_{k,l} = 1 - \text{mean}\left(\left|\overrightarrow{\text{submatrix}(\mathbf{X}, k, k + r_0 - 1, l, l + r_0 - 1) - \mathbf{W}^m}\right|\right)$, nonlinear processing by the expression $\text{EN}^m_{k,l} = G\left(a, E^m_{k,l}\right) = 0,5\left[1 + \left(2E^m_{k,l} - 1\right)^a\right]$, and comparing each other to determine the winners for indexing expressions: $\text{MAX}_{k,l} = \underset{\text{index } m}{\max}\left(\text{EN}^{m=0}_{k,l}, \text{EN}^{m=1}_{k,l} \ldots \text{EN}^{M-1}_{k,l}\right)$ and $\text{EV}^m_{k,l} = f^{\text{activ}}_{\text{nonlinear}}\left(\text{EN}^m_{k,l}, \text{MAX}_{k,l}\right)$. Thus, in the first and second steps, it is necessary to calculate a large number of convolutions.

From the above formulas, it follows that it is necessary to calculate the average value of the component-wise difference of two matrices. Similarly, normalized nonequivalent functions for all filters are calculated, and their components are nonlinear transformed: $\mathbf{EN}0_{k,\,l} = 0.5[1 + (2\mathbf{E}0_{k,\,l} - 1)^{\alpha}]255$, where α is the

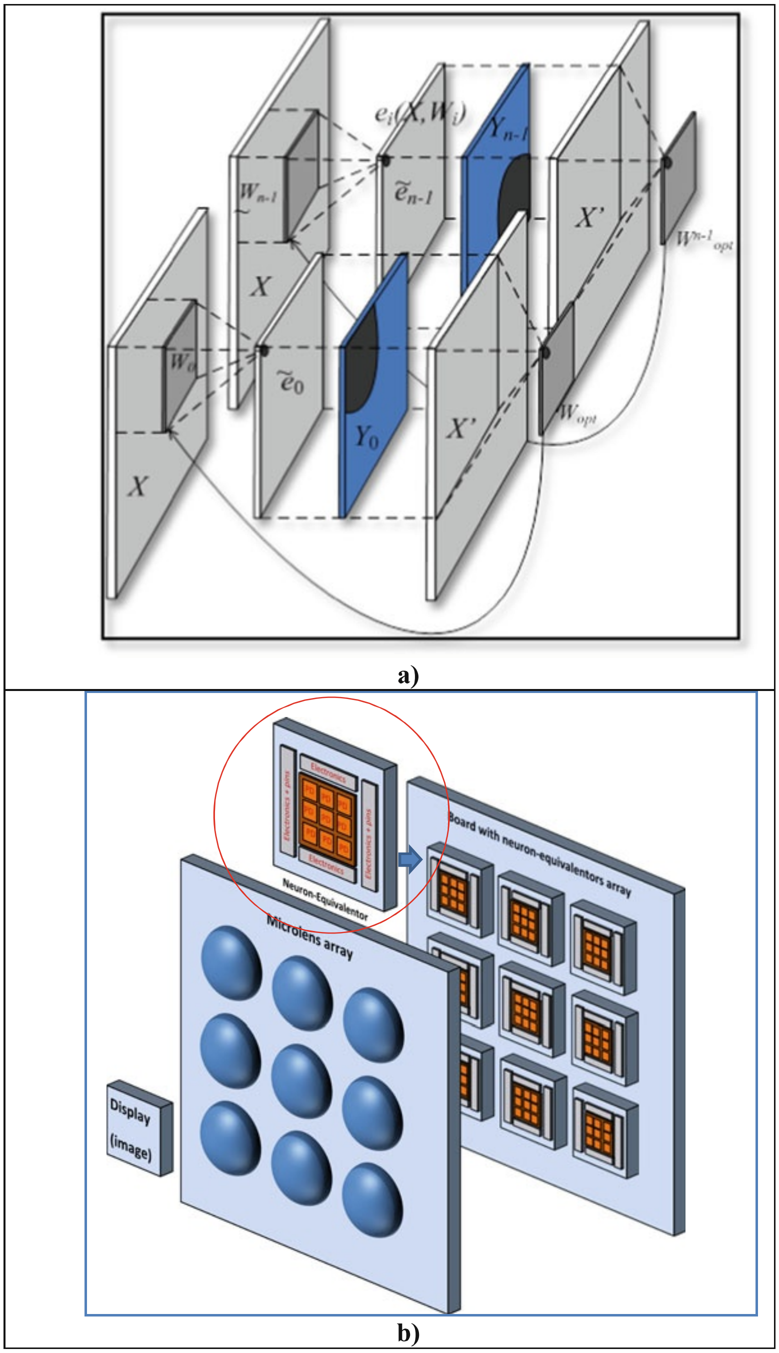


Fig. 4.1 The basic unit (structure) of the SLECNS, which explains the principle of its functioning of learning neural network model based on the multi-port memory to find centroid cluster elements (**a**); the basic unit that uses an array of neuron equivalentors (**b**)

nonlinearity coefficient. Based on these transformations for SLECNS, we need to implement nonlinear transformations for different α. The analysis of this expression shows that it is necessary to rise to power and multiply, so we propose to approximate this dependence, for example, by three-piece linear approximation. The experiments conducted in work [26] show great promise of the proposed methods and models of self-learning recognition of images, including multilevel and color images. But for their work in real time, taking into account the large requirements for performance and the amount of calculations, it is necessary to have appropriate high-performance and energy-efficient arrays and image processors with parallel principles of operation and picture input-outputs, whose design was partially considered in papers [9, 12, 13, 58–64]. In Fig. 4.1b a new structure proposed by us in [65] is shown, which may be promising for use in machine vision and artificial intelligence, neural structures, in various high-performance measurement systems [66–68]. The presented structure makes it possible to calculate in parallel the set of all components (elements) of the equivalent convolution at once in a single cycle at high speed. The cycle time is equal to the time of selection from the processed image of its shifted current fragment. The structure of the system that uses an array of neuron equivalents consists of a microdisplay that dynamically displays the current fragments, an optical node as an array of microlenses (MLA) with optical lenses (not shown!), and a two-dimensional array of equivalentors (Eqs) with optical inputs. Each Eq is implemented in a modular hierarchical manner and can consist of similar smaller sub-pixel, also 2D-type, base nodes. The equivalentor has a matrix of photodetectors, on which a halftone image of a fragment is projected using (MLA). The number of electrical analog inputs is equal to the number of photodetectors, to which the filter components are fed from a sampling and holding device (SHD) or analog memory with subsequent digital-analog conversion using any known method.

These components are presented in the form of microcurrents. Each equivalentor has its own filter mask from the filter set, which is formed as a result of training. Simulation on 1.5 µm CMOS transistors in various modes showed that such equivalentors and their basic blocks can operate in low-power and high-speed modes, their energy efficiency is estimated to be at least 10^{12} an. op/sec per watt and can be increased by an order of magnitude, especially considering FPAA [69]. But much depends on the accuracy of the current mirrors and their characteristics. Thus, at the inputs of each equivalentor, there are two arrays (vectors) of analog currents representing the current fragment being compared and the corresponding filter standard, and the output of the equivalentor is an analog current signal that is nonlinearly transformed in accordance with the activation function and represents a measure of their similarity, proximity. Also, as have been shown [65], nonlinear component-wise transformations allow even without WTA network to allocate the most NEs with the greatest activity. From the above described, it follows that for hardware implementations of all the advantages of SI EM, an important issue is the design of parallel nonlinear transformations, transformations of intensity levels. And, as will be shown below, the use of an array of cells that perform hardware and not with PC, nonlinear transformations adequate to auto-equivalence operations, allows the laborious computational process of searching for extremums in SD_NEF (maps for clustering and learning) not to be performed, but to automatically select these extremums using only several transformation steps and eliminate all unnecessary levels, making these level pixels neutral for subsequent algorithmic steps.

4.2.2 Brief Review and Background of Mathematical Operators, Which Are Implemented by Neurons

Almost all concepts, models, and structures of NN and CNN use informational mathematical models of neurons, which are reduced to the presence of two basic mathematical component operators: the first component computes a function from two vectors $\overrightarrow{X}$ and $\overrightarrow{W}$, where $\overrightarrow{X}$ is the vector of input signals of a neuron, $\overrightarrow{W}$ is the vector of weights, and the second component corresponds to some nonlinear transformation of the output value of the first component to the output signal. The input operator can be implemented as sum, maximal or minimum value, a product of the self-weighted inputs [55, 56]. But recently, the set of such operators has expanded significantly [6, 9, 13, 56]. Equivalence models of neural networks, which have some advantages, require the computation of such operators: normalized equivalence (NEq), nonlinear normalized nonequivalence (NnEq), and autoequivalence of vectors. In [9, 13, 57], we considered how to implement these input operators for the case when the components of the vectors $\overrightarrow{X}$ and $\overrightarrow{W}$ are both normalized and unipolarly encoded. In work [58], we used just normalized equivalences, but time-pulse coding was used for analog signals. The positive aspect of that work was the use of a modular principle that allowed the calculation of the operator of the normalized equivalence of a vector to the calculation of normalized equivalent subvectors and their output signals. In paper [58], the mathematical basis of the creation of neurons of equivalents calculating the function of NEq is described in detail, using the modular principle. To increase the number of inputs of our complementary double NE (CDNE) or the dimension of the compared vectors, you can use the combination of the basic analog CDNE of a smaller dimension. This greatly expands the functionality of such a basic CDNE, especially when they are combined in complex hierarchical structures. It shows that all algorithmic procedures in the equivalence paradigm of NNs and AM on their basis are reduced to the calculation of NEqs from two vectors or matrices, and the elemental nonlinear transformations that correspond to the activation functions, and for the above EMs of NNs, reduce to the calculation of auto-equivalences (auto-non-equivalences). But in the above works, activation functions were not simulated and shown. A lot of work has been devoted to the design of hardware devices that realize the functions of activation of neurons, but they do not consider the design of exactly the auto-equivalent transformation functions for EMs and the most common arbitrary types and types of nonlinear transformations. Therefore, the goal of this paper is the design of cells for hardware parallel transformation of image intensity levels. In work [65], the question of the simplest approximations of auto-equivalence functions (three-piece approximation with a floating threshold) was partially solved. The basic cell of this approximation consisted of only 18–20 transistors and allowed to work with a conversion time from 1 to 2.5 µs. At the same time, the general theoretical approaches to the design of any nonlinear type of intensity transformation were not considered, and this is the objective of the paper. The operations of addition and subtraction of currents are most easily performed on current mirrors.

4.2.3 Mathematical Models of Nonlinear Transformations of Image Intensities

The input analog intensity of the pixel is denoted by x, where $x \in [0, D]$, D is the maximum intensity of the selected range, and denotes the output analogized transformed intensity by y, where $y \in [0, D]$. Then the operator of the nonlinear intensity transformation can be written in the form: $y = F_{\text{trans}}(x)$. As such functions can be threshold processing functions, exponential, sigmoid, and many others, which, in particular, are used as activation functions in the construction, synthesis of neural elements and networks are based on them. To form the required nonlinear intensity transformations, it is possible to use a piecewise linear approximation of the chosen functions. For a piecewise-linear approximation, break the range of input levels D into N equal sub-bands, width $p = D/N$. Using the function of bounded difference known from papers [6, 13], defined as $a \dot{-} b = \begin{cases} a - b, & \text{if } a > b \\ 0, & \text{if } a \le b \end{cases}$. Form for the input signal x and each upper sub-band level $pD_i = i \cdot p$, where $i = 1 \ldots N$, the following signals: $s_i = \left(x \dot{-} (i-1)\,p\right) \dot{-} \left(x \dot{-} i \cdot p\right)$. For $i = 1$ we get $s_1 = x \dot{-} \left(x \dot{-} p\right)$, and this is the minimum $\min(x, p)$, and there is a step signal with height p. For $i = 2$ we get $s_2 = \left(x \dot{-} p\right) \dot{-} \left(x \dot{-} 2p\right)$, which corresponds to a step in height p, but which begins at p. For $i = N$ we get $s_N = \left(x \dot{-} (N-1)\,p\right) \dot{-} \left(x \dot{-} N \cdot p\right) = \left(x \dot{-} (N-1)\,p\right)$, which corresponds to a step in height p, but which begins at $(N-1)p = D - p$. Summing with the weight coefficients k_i of these steps, we can form a piecewise approximated intensity.

$$y_a = \sum_{i=1}^{N} k_i s_i = \sum_{i=1}^{N} k_i \left[\left(x \dot{-} (i-1)\,p\right) \dot{-} \left(x \dot{-} i \cdot p\right)\right], \tag{4.2}$$

For forming $y_a \in [0, D]$, that is, the normalized range of its levels, the weighting coefficients of the steps are selected from the condition: $\sum_{i=1}^{N} k_i = N$. Analysis of formula (4.1) shows that by changing the gain of the steps, we can form any required piecewise continuous intensity conversion function. If the coefficient k_i is negative, it means that the corresponding step is subtracted. Thus, in order to implement the transformations, a set of nodes for realizing operations of bounded difference, weighting (multiplication), and simple summation are needed. If the input pixel intensity is set by the photocurrent, then having the current mirrors (CM), by which the operations of the limited difference and the summation of the photocurrents are easily realized, it is sufficient to have a plurality of limited difference schemes and the specified upper sub-band levels pD_i. By choosing the parameters of the current mirror transistors, operations of dividing or multiplying are currents by the required fixed k_i. If it is necessary to dynamically change the view, the conversion function, that is, the weight of the components, then you need the coded amplifiers. When working with currents and CM, a set of keys and a multiplying mirror with discrete weights (binary) perform the role of code-controlled amplifiers and are essentially DAC with the only difference that instead of a reference analog signal, an analog signal s_i. After some transformations, formula (4.2) is transformed into this form:

$$y_a = \sum_{i=1}^{N} k_i \left[\left(x \dot{-} pD_{i-1} \right) \dot{-} \left(x \dot{-} pD_i \right) \right] = \sum_{i=1}^{N} k_i \cdot \min \left(x \dot{-} pD_{i-1}, p \right) \tag{4.3}$$

Formula (4.3) indicates that for the implementation of the intensity conversion, it is necessary to have analogous minimum circuits, but it is realized in the form of two operations of bounded difference: $a \dot{-} \left(a \dot{-} b \right) = \min(a, b)$. In addition to the formulas (4.2) and (4.3) considered above, it is possible to realize the required function by means of triangular signals:

$$y_a = \sum_{i=1}^{N} k_i \cdot t_i = \sum_{i=1}^{N} k_i \left[\left(x \dot{-} (i-1) \cdot p \right) \dot{-} 2 \left(x \dot{-} i \cdot p \right) \right] \tag{4.4}$$

For the formation of the constants s_i or t_i, the input signal x can be multiplied by N, and then all components are simultaneously generated simultaneously in each sub-assembly. On the other hand, in each sub-assembly, a signal $\left(x \dot{-} pD_i \right)$, this is fed to the next in the pipeline sub-assembly for the formation of signals and components from it. This corresponds to a conveyor circuit that will have a large delay but does not require the multiplication of the input signal. The choice of this or that scheme and element base depends on the requirements for the synthesized node.

4.2.4 Simulation of Array Cells for Image Intensity Transformation

4.2.4.1 Simulation of Image Intensity Transformation with Mathcad

Using both the basic components for the composition of the lambda function **fspΔs2**, shown in Fig. 4.2 and described by expression:

$$\mathbf{fsp\Delta s2}\left(\mathbf{xs}, \mathbf{p\Delta x}, \mathbf{p\Delta}, \mathbf{k}\right) = \mathbf{k} \times \mathbf{obs}\left(\mathbf{obs}\left(\mathbf{xs}, \mathbf{p\Delta x}\right), \mathbf{obs}\left(\mathbf{xs}, \mathbf{p\Delta}\right) \times \mathbf{2}\right) \tag{4.5}$$

where **xs** is the function argument, **pΔx** is the parameter indicating the lower bound level **xs** (beginning), **pΔ** is the second parameter indicating the level for the maximum, k is the third parameter indicating the scalar gain multiplier; and abs $(a, b) = a \dot{-} b$, we proposed a function composition **fspΔsS**, which is calculated by the expression:

$$\mathbf{fsp\Delta sS}\,(\mathbf{xs}, \mathbf{\Delta k}, \mathbf{VK}) = \sum_{\mathbf{i=1}}^{\mathbf{\Delta k}} \mathbf{fsp\Delta s2}\left[\mathbf{xs}, \frac{\mathbf{255}}{\mathbf{\Delta k}} \times (\mathbf{i}-\mathbf{1}), \frac{\mathbf{255}}{\mathbf{\Delta k}}(\mathbf{i}), \mathbf{VK_i}\right] \tag{4.6}$$

where **Δk** is the number of components (lambda functions), **xs** is the argument of the function, and **VK** is the vector of gain factors. The result of constructing some types of transfer characteristics (TC) using these functions in the Mathcad environment is shown in Fig. 4.2. To approximate auto-equivalence, we also offer simpler (two-step) basic N-functions:

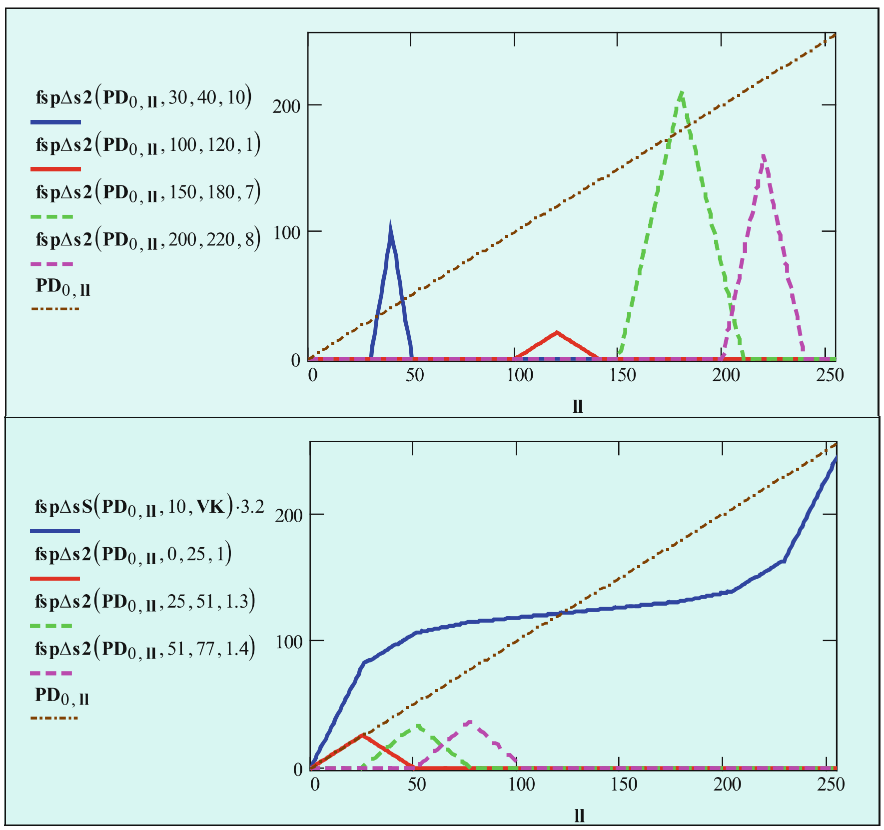


Fig. 4.2 Graphs of synthesized transformation functions

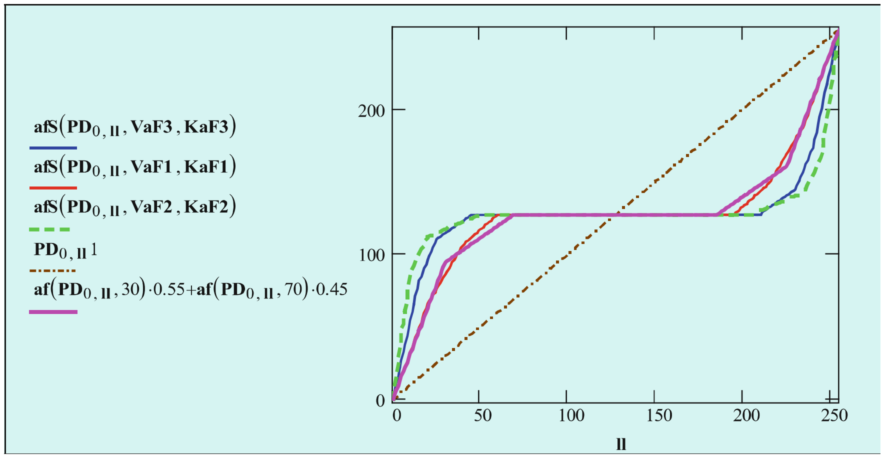


Fig. 4.3 Examples of synthesized transfer characteristics for auto-equivalence functions

$$\mathbf{af}\,(\mathbf{xs}, \mathbf{xp}) = [\mathbf{obs}\,(\mathbf{xs}, \mathbf{obs}\,(\mathbf{xs}, \mathbf{xp})) + \mathbf{obs}\,(\mathbf{xs}, (\mathbf{DP} - \mathbf{xp}))] \cdot \left(\frac{\mathbf{DP}}{\mathbf{xp} \cdot \mathbf{2}}\right) \tag{4.7}$$

and triple their composition:

$$\mathbf{afS}\,(\mathbf{xs}, \mathbf{VaF}, \mathbf{KaF}) = \sum_{\mathbf{iv}=\mathbf{0}}^{\mathbf{2}} \mathbf{af}\,(\mathbf{xs}, \mathbf{VaF_{iv}}) \cdot (\mathbf{KaF_{iv}}) \tag{4.8}$$

In general, the number of components in a composition can be arbitrary, but for modeling we used 8- and 16-component compositions and adjustment vectors. Examples of such functions and compositions for the synthesis of TC are shown in Fig. 4.3. Another variety of functions is shown in Fig. 4.4, and the results of using such TCs to prepare the original PIC image are shown in Fig. 4.5.

4.2.4.2 Design and Simulation of Array Cells for Image Intensity Transformation Using OrCad PSpice

Let us first consider the design and simulation of a single base cell for the image intensity of an arbitrary transformation, using the example of a four-piece approximation by triangular signals according to formula (4.4). Figure 4.6 shows the scheme used for modeling, and Fig. 4.7 shows the schematic of the basic sub-node. To form four triangular signals from the input signal, we use four identical sub-nodes, each of which consists of 14 (13) transistors and an additional current mirror (two transistors Q18 and Q19), and for propagation of the input photocurrent and threshold levels, the auxiliary circuit consists of 17 (14) transistors.

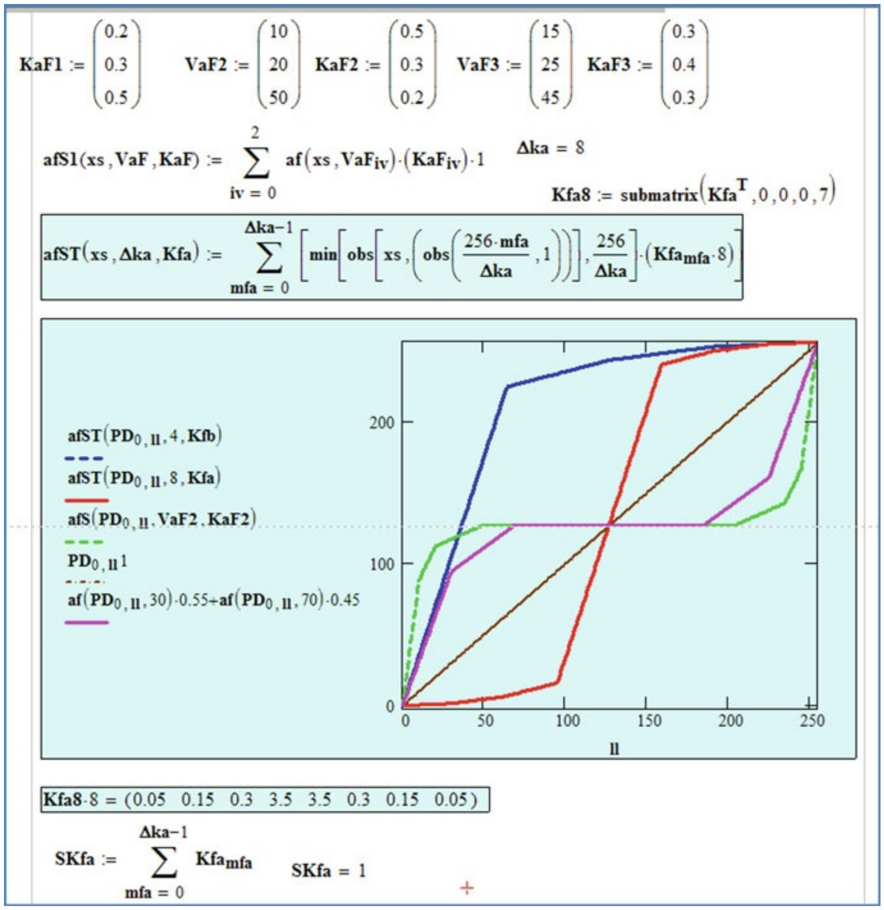


Fig. 4.4 Mathcad windows with the formulas and graphs of synthesized transformation functions

The input photocurrent was simulated by a current generator I2. In general, the cell layout consists of 68 transistors. In this scheme for simulation, we used four fixed different gain values for each triangular signal. To do this, the output signal of the sub-node was multiplied using the current multiplier mirror (CMM), and by fixing the output connections S0–S3 with the summing output current mirror or the power line, we chose the weights k_i. Thus, we modeled different transformation functions by choosing a set of coefficients k_i. The simulation results for various input signals are shown in Fig. 4.8.

Using a linearly increasing input signal (red solid line) and a conversion function, the form of which is shown in the green bold line in Fig. 4.8a, and using auxiliary signals (shown in different colors), we obtained a nonlinear transformation similar to the ReLu function (with saturation). In Fig. 4.8b, the resultant signal (green bold line) is shown after a nonlinear conversion by means of this function of the input

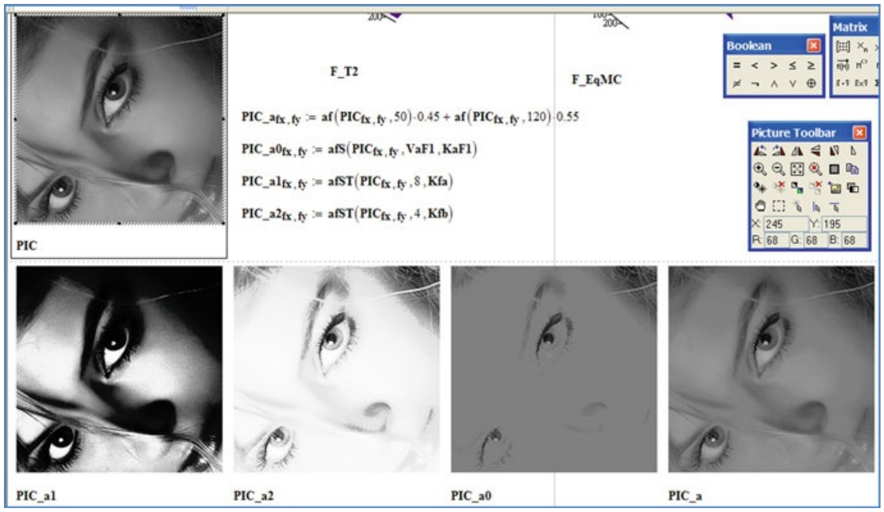


Fig. 4.5 Mathcad windows on which the formulas and results of image intensity transformation are shown, wherein 2D from left to right: input image PIC, the computed auto-equivalence functions, nonlinear (after activation) output images (bottom row)

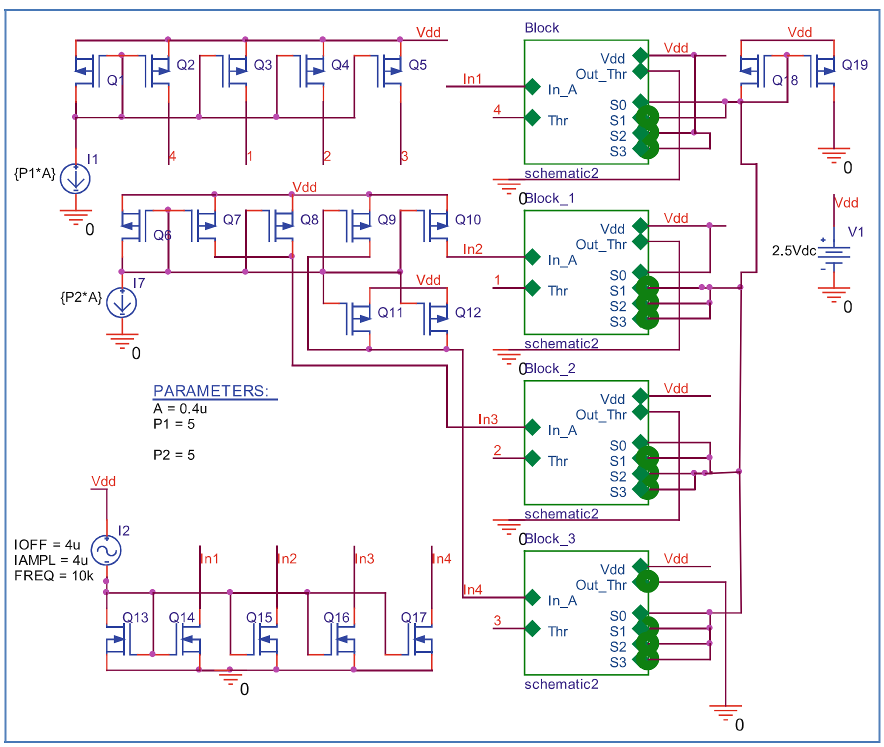


Fig. 4.6 Circuit for simulation of nonlinear converter cell on the base of four-piece linear approximation and four base sub-nodes

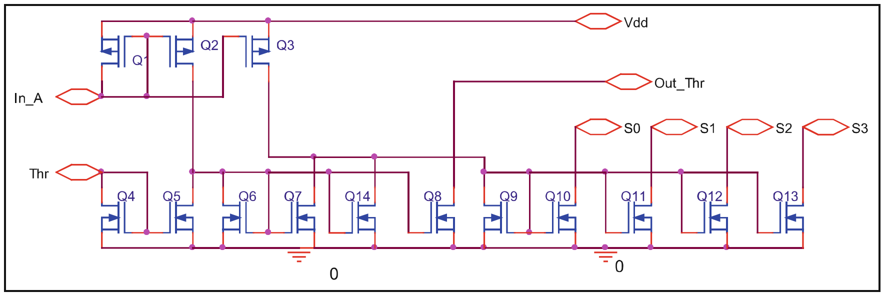


Fig. 4.7 Circuit of base sub-node (schematic 2) for four-piece linear approximations

sinusoidal signal (shown in blue). The power consumption of the cell is 150 μW at a supply voltage of 2.5 V, Imax $= D = 8$ μA, $N = 4$, $p = 2$ μA, and the periods of the input signals are 200 and 100 μs. To dynamically switch the view of the image pixel intensity conversion function, we use the current-controlled current amplifiers on current mirror multipliers (CCCA) with binary-weighted current outputs (Fig. 4.9). The general scheme of the cell realizing the dynamic intensity conversion with eight piecewise linear approximation is shown in Fig. 4.10. This circuit contains 170–200 transistors and consists of eight basic nodes (A + CCCA). The Node A consists of 8 (7) transistors and generates a triangular signal from the input signal at a given threshold for each sub-band pD_i. The auxiliary circuits for generating upper sub-band levels and subtracting them from the input signals are shown at the left in Fig. 4.10 and can be implemented in different ways depending on the selected element base and approach. The processes of formation from the input signal of all auxiliary components, triangular waveforms, nonlinearly transformed output signal, and simulation results of this circuit for different modes are shown in Figs. 4.11 and 4.12. For a supply voltage of 2.5 V, Imax $= D = 8$ μA, $N = 8$, $p = 1$ μA and the period of the input linearly increasing-decreasing triangular signal equal to 1000 μs.

Removing only one transistor in node A of the circuit in Fig. 4.10 allows it to modify and implement on the basis of tunable nonlinear transformations in accordance with the formula (4.1), and not (4.3), that is, with the help of s_i, but not t_i.

The results of modeling such as conversion scheme with the composition of the basic step signals s_i are shown in Figs. 4.13, 4.14, and 4.15, and Figs. 4.14 and 4.15 show the case of four-level approximation and Fig. 4.13 the eight-level approximation. The results confirm the possibility of synthesizing converter cells with specified or required accuracy characteristics of the transformation laws and, in particular, auto-equivalence functions, the microvolt level of power consumed by them, and high speed (microseconds and less). For the simplest and approximate approximation functions, but often quite sufficient for the selection of the winning function by the activation function, the cell circuits consist of only 17–20 transistors, have a very high speed ($T = 0.25$ μs), and a small power consumption (less than 100 μW). The results of simulating such simple (3–4 piecewise approximation) cells

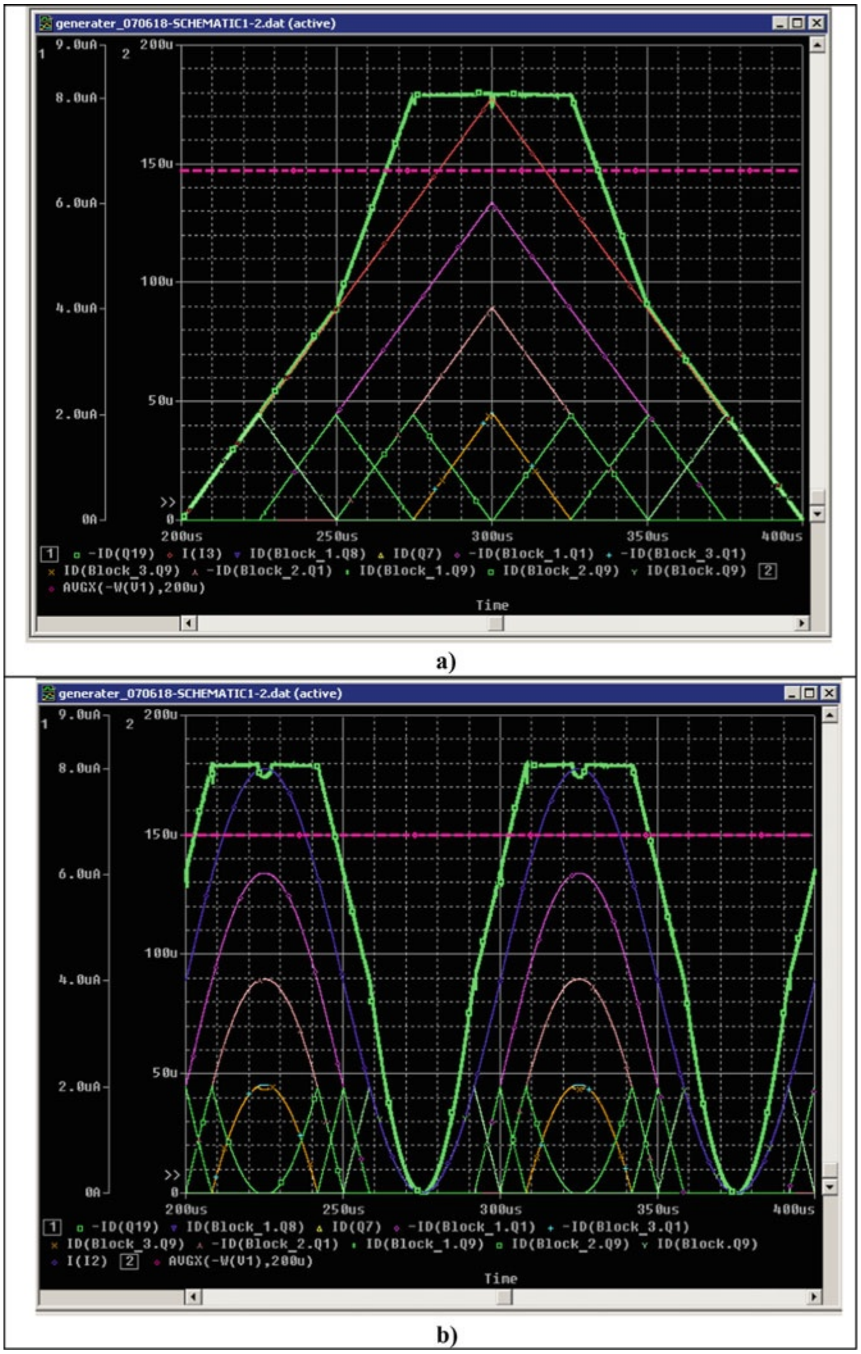


Fig. 4.8 Simulation result for the circuit in Fig. 4.6 for input linear rising signal (**a**) and for input sinusoidal signal (**b**)

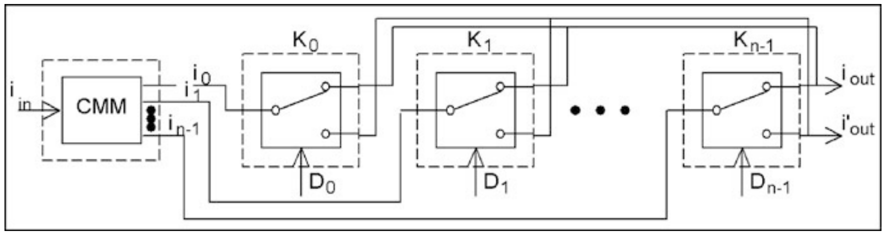


Fig. 4.9 Code-controlled current amplifier (CCCA) that consists of current mirror with multiplication (CMM) and set of *n* keys (*K*)

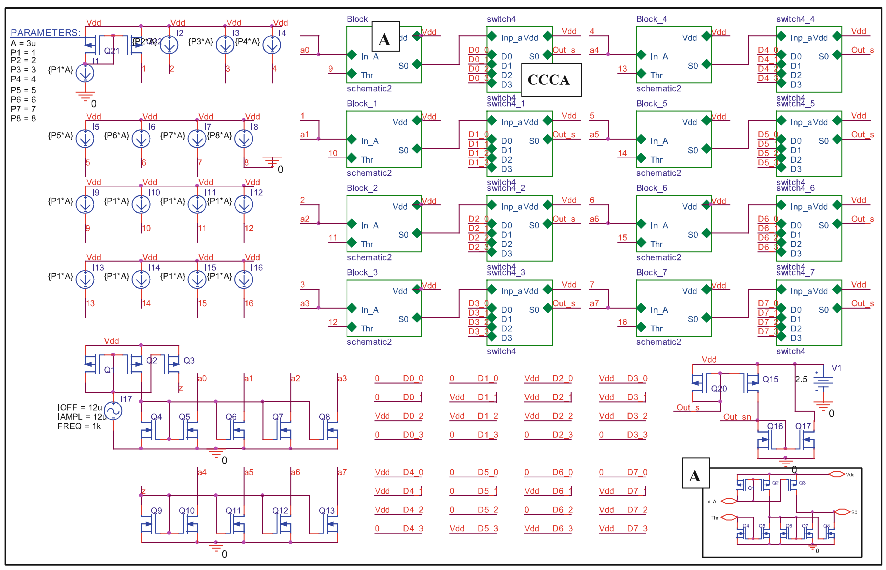


Fig. 4.10 Circuit for simulation of nonlinear converter cell on the base of eight-piece linear approximation and eight base sub-nodes

(see Fig. 4.16) separately and in the composition with nodes for input operators, and in small-sized networks of Eq equivalents are presented in Sect. 4.2.4.3 and are shown in Figs. 4.17 and 4.18. The analysis of the obtained results confirms the correctness of the chosen concept and the possibility of creating CLCs for image intensity transformation and MIMO structures on their basis, as hardware accelerators for compact high-performance systems of machine vision, CNN, and self-learning biologically inspired devices.

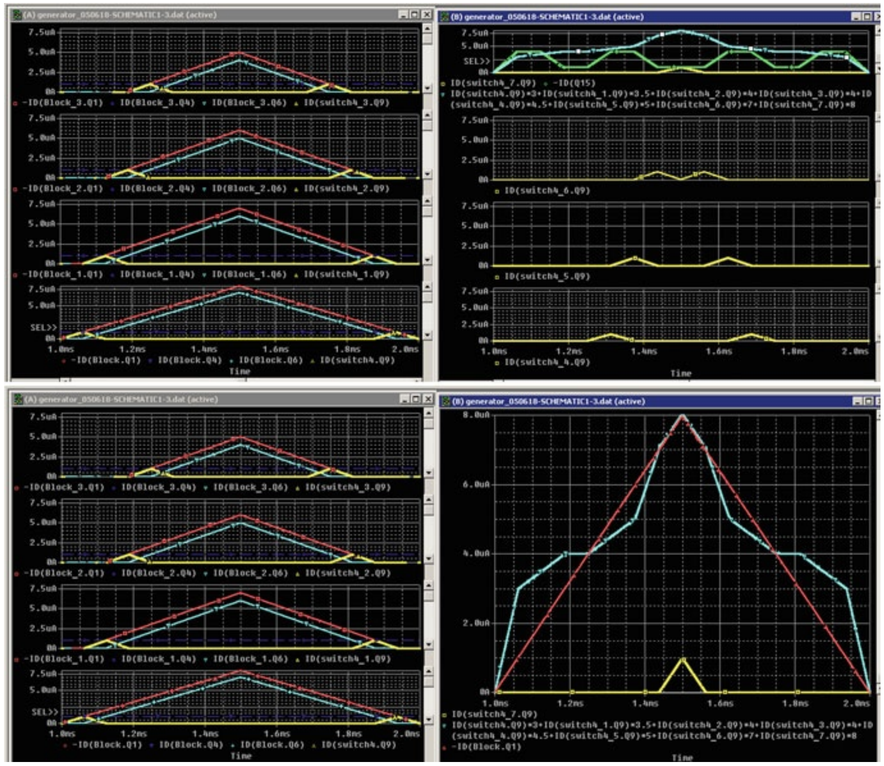


Fig. 4.11 Simulation result for eight sub-node circuit (Fig. 4.10): up left, formation of triangle signals for linear rising input signal (red line), output signal (yellow line) (the first four signals); up right, formation of triangle signals (red line), output signal (yellow line) (the second 4 signals) and two outputs for two characteristics (blue and green lines); down right, input signal (red line), output signal (blue line)

4.2.4.3 Simulation of Nonlinear Transformation in Analog 64-Input and 81-Input Neuron Equivalentor

For the simulation of nonlinear transformation in analog 64-input and 81-input neuron equivalentor [65], we used a node whose circuit is shown in Fig. 4.16, which forms the activation function (autoequivalence) in the form of a piecewise linear approximation. Simulating results of such 64-input NE with the nonlinear conversion of the output signal response for linearly rising (falling) currents with a period $T = 2.5\ \mu s$ are shown in Figs. 4.17 and 4.18. In the same place, the results of modeling the formation processes of linear and nonlinear normalized NEq are shown. Comparing two vectors with current signals, the 64-input neuron equivalent has a total power consumption of approximately 2–3 mW at a low supply voltage, contains less than 1000 CMOS transistors, and provides good temporal characteristics.

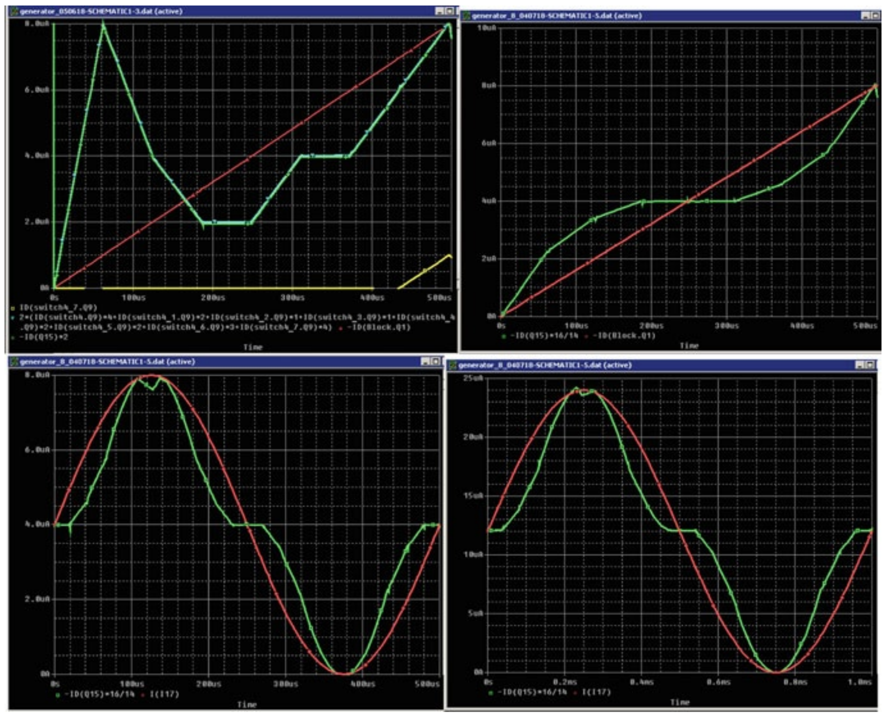


Fig. 4.12 Simulation result for eight sub-node circuit (Fig. 4.10): up left, for linear rising input signal (red), output signal (green), and corresponds to N-shape transfer characteristic; up right, for linear rising input (red), output signal (green), and corresponds to the auto-equivalence transfer characteristic; down left and right, for sinusoidal input signal (red), output signal (green), and corresponds to the auto-equivalence transfer characteristic for input current range 0–8 μA and period 500 μs (down left graph), 0–24 μA, and 1 ms (down right graph)

The circuit performs summation, limited subtraction, and multiplication of analog currents on current mirrors.

4.3 Continuous-Logic (CL) Transformation and the Equivalently CL ADC

4.3.1 Basic Theoretical Foundations, Equivalence Models, and Their Modification for SMC_CL_ADC

These converters significantly reduce (or even eliminate) the error of digitization (quantization) inherent in the classical ADC. The CL transformations are given in [30, 45, 51], in which the transformation CL functions (CLF) are defined, and it is

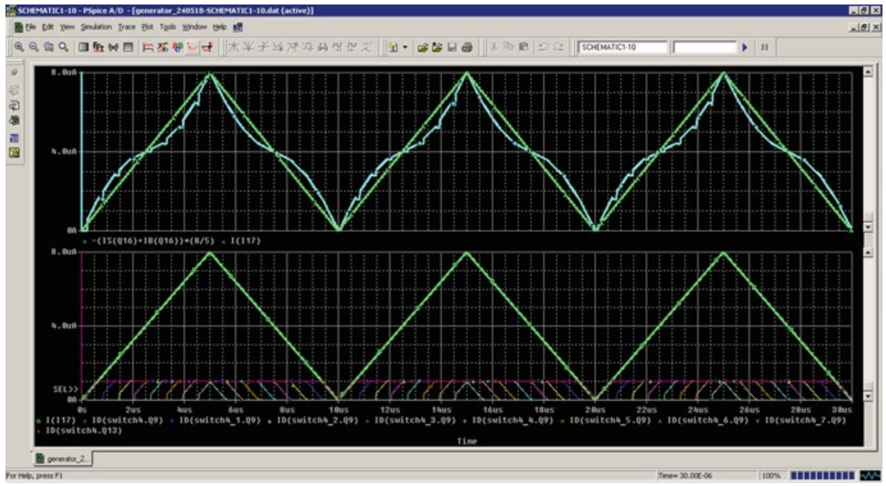


Fig. 4.13 Simulation result for circuit with step signals and eight-level approximation of input current signal: input signal (green line), output signal (blue line), and other signals (color lines)

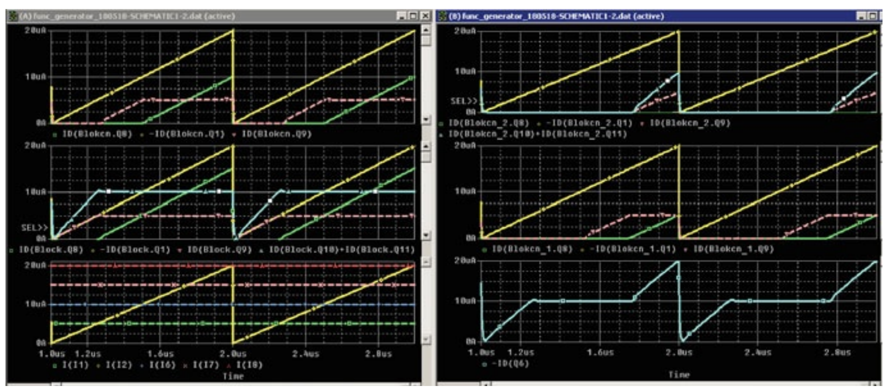


Fig. 4.14 Simulation result for four-level approximation, the realized nonlinear transformation is the normalized auto-equivalence function for self-learning convolutional networks (Imax $= 20\ \mu$A, $T = 1\ \mu$s)

shown that the operation of min and max of continuous logic are the basic operations of the functions. Using operators of hybrid logic for the formation of CLF, it is possible: $D_1[P(x1, x2)] = \max(x_1, x_2)$, $D_2[P(x1, x2)] = \min(x_1, x_2)$ where P and D are, respectively, threshold and non-threshold operators, which are implemented in various ways. In many models of neural networks for image recognition, especially many graded ones, it is desirable to have binary bit-plane images that encode the image matrix in Gray codes [41]. In addition, in a number of works [32–35, 40, 45, 46], it was shown that some operations of continuous logic, such as equivalence and nonequivalence, and their generalized family, provide a number of advantages in the

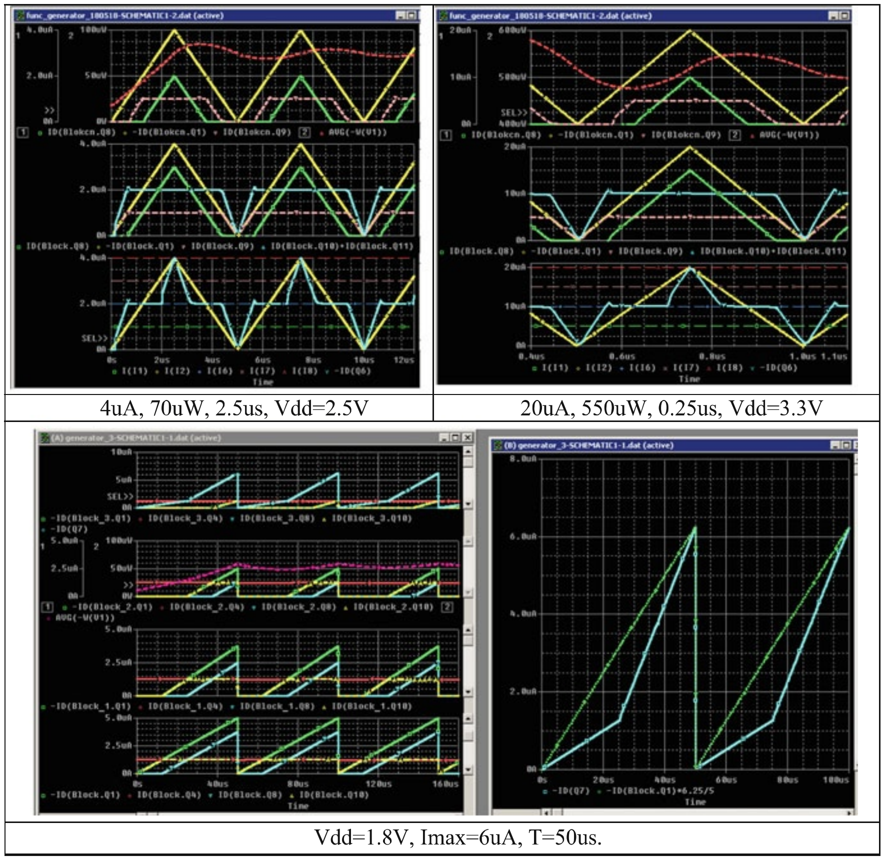


Fig. 4.15 Simulation result for four-level approximation, the realized nonlinear transformation is the normalized auto-equivalence function for self-learning convolutional networks (for different input currents and transformation periods): input signal (yellow line), output signal (blue line), and power consumption (red line)

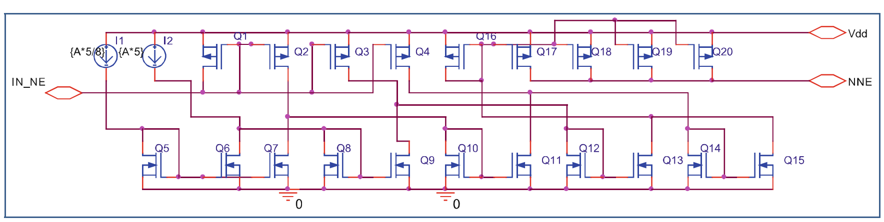


Fig. 4.16 Activation function circuit on current mirrors

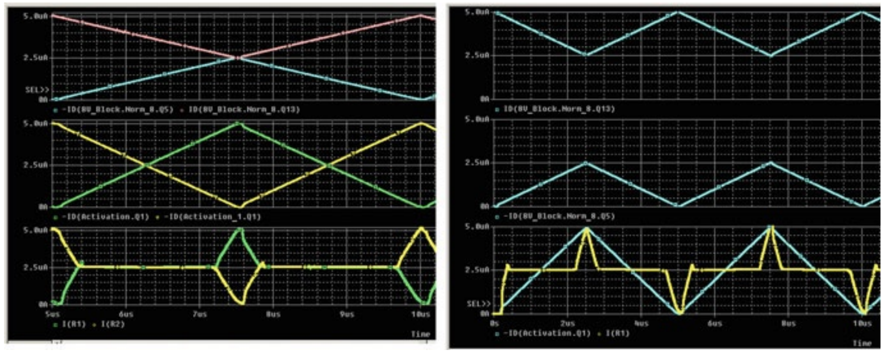


Fig. 4.17 The results of modeling the 64-input Eq for current Imax = 5 μA, and a linearly rising (falling) currents with a period $T = 2.5$ μs. On the left two upper signals (pink, maximum; blue, minimum of two input currents), green, equivalent signal; yellow, nonequivalence, below the signals after their nonlinear conversion; on the right, the two upper signals are the maximum and minimum, the lower blue is the normalized equivalence, the yellow is the nonlinear normalized equivalence

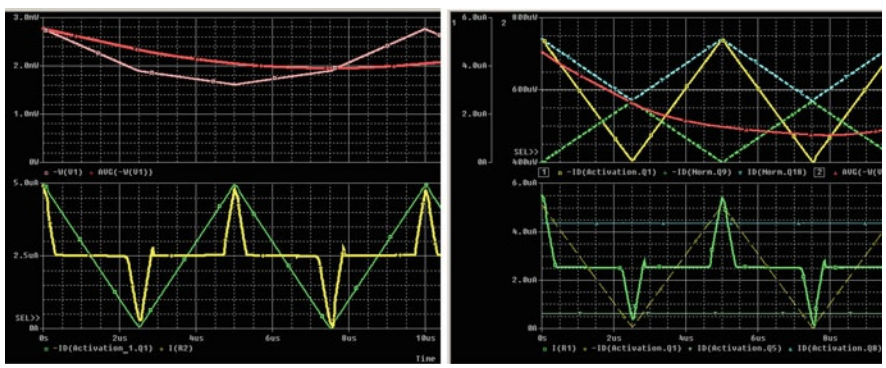


Fig. 4.18 The results of modeling the 64-input Eq for current Imax = 5 μA, and a linearly rising (falling) currents with a period $T = 2.5$ μs. On the left: the results of modeling the processes of formation of linear (green) and nonlinear normalized NEqs (yellow); on the upper graph: the peak and average consumption powers; on the right: the results of modeling the processes of formation of linear (yellow on the upper trace) and nonlinear normalized NEqs (green on the bottom trace), red line shows the power of consumption. Blue, maximum of two signals; green, minimum of two signals for $V = 3.3$ V

so-called equivalence paradigm. These scalar operations of equivalence eq(x,y) and nonequivalence neq(x,y) for x, $y \in [0,1]$ are defined in papers [32, 33], namely

$$\mathrm{eq}\,(x, y) = x \wedge y + \overline{x} \wedge \overline{y} = \min\,(x, y) + \min\,((1 - x)\,, (1 - y)) = 1 - |x - y| \tag{4.9}$$

$$\begin{aligned} \mathrm{neq}\,(x, y) = |x - y| = 1 - \mathrm{eq}\,(x, y) = \max\,(x, y) - \min\,(x, y) \\ = \max\,(\overline{x}, \overline{y}) - \min\,(\overline{x}, \overline{y}) = \left(x \dot{-} y\right) + \left(y \dot{-} x\right) \end{aligned} \tag{4.10}$$

where $(\dot{-})$ is the limited difference operation. If we consider it for $y = 1\dot{-}x = \overline{x}$, these functions are transformed to:

$$\mathrm{eq}\,(x, \overline{x}) = 2\,(x \wedge \overline{x}) = 2 \min\,(x, \overline{x}) \tag{4.11}$$

$$\mathrm{neq}\,(x, \overline{x}) = \max\,(x, \overline{x}) - \min\,(x, \overline{x}) = 1 - 2 \min\,(x, \overline{x}) \tag{4.12}$$

As it has been shown in work [45], these functions can be successfully used in the CL ADC. For the formation of binary bit planes that correspond to the categories of images coded in the Gray code, we used for each pixel an iterative procedure over the matrices of equivalence and nonequivalence obtained in the previous stages:$\mathrm{eq}_{i+1}(\mathrm{eq}_i(\ldots), \mathrm{neq}_i(\ldots))$ and $\mathrm{neq}_{i+1}(\mathrm{eq}_i(\ldots), \mathrm{neq}_i(\ldots))$. It is easy to see that the division of the segment [0, 1] into $2^n = N$ subranges sets each of them a set, a vector of signs, which corresponds to the Gray code measured by the scalar size x. Thus, positional digit d_{n-i} of the code is defined as

$$d_{n-i}\left(\mathrm{eq}_{i-1}, \mathrm{neq}_{i-1}\right) = \left\{1, \text{ if } \mathrm{eq}_{i-1} > \mathrm{neq}_{i-1}, \ 0, \text{ if else}\right\} \tag{4.13}$$

where $i \in 1 \ldots n$, and $\mathrm{eq}_0 = x$, $\mathrm{neq}_0 = \overline{x}$. From this, it is obvious that in order to realize the ADC for optical signals, we needed to synthesize BC CLs that implement the required operations eq_i, neq_i and the threshold operators. We called such ADCs equivalent to continuously logical, complementary dual ones, since the signals x and $\overline{x}$ in them are complementary, and the CL functions are equivalent (nonequivalent), that is, equivalently CL ADC [45]. Since these ADCs were implemented on current mirrors (CM), and the input signals of the ADC are currents, we will designate such an ADC as an ADC CM [30]. In this work, as transformation CLFs, we use the following functions:

$$\begin{array}{l} \mathrm{eq}_{i+1}\left(\mathrm{eq}_i, D/2\right) = 2\left(\mathrm{eq}_i \dot{-} 2\left(\mathrm{eq}_i \dot{-} D/2\right)\right) \quad \text{or} \\ \mathrm{neq}_{i+1}\left(\mathrm{neq}_i, D/2\right) = 2\left|\mathrm{neq}_i - D/2\right| \end{array} \tag{4.14}$$

where $\mathrm{eq}_0 = x$, $\mathrm{neq}_0 = \overline{x}$, which allow us to work not with two signals, but with one signal, thereby simplifying the implementation of the cells. Structure of SMC CL ADC for IP is shown in Fig. 4.19.

4.3.2 Design of CL ADC CM-6 (8) (G): iv (the Iteration Variant) Based on DC-(G) (with Gray Code)

Figure 4.20 shows a circuit of one channel of SMC_ADC. The structure is shown in Fig. 4.20a and the base cell in Fig. 4.20b. The circuit consists of a sample and hold device (SHD), a single digital-analog DC-(G) cell (block A), and additional elements (block B). The input analog current signal to be converted is recorded in

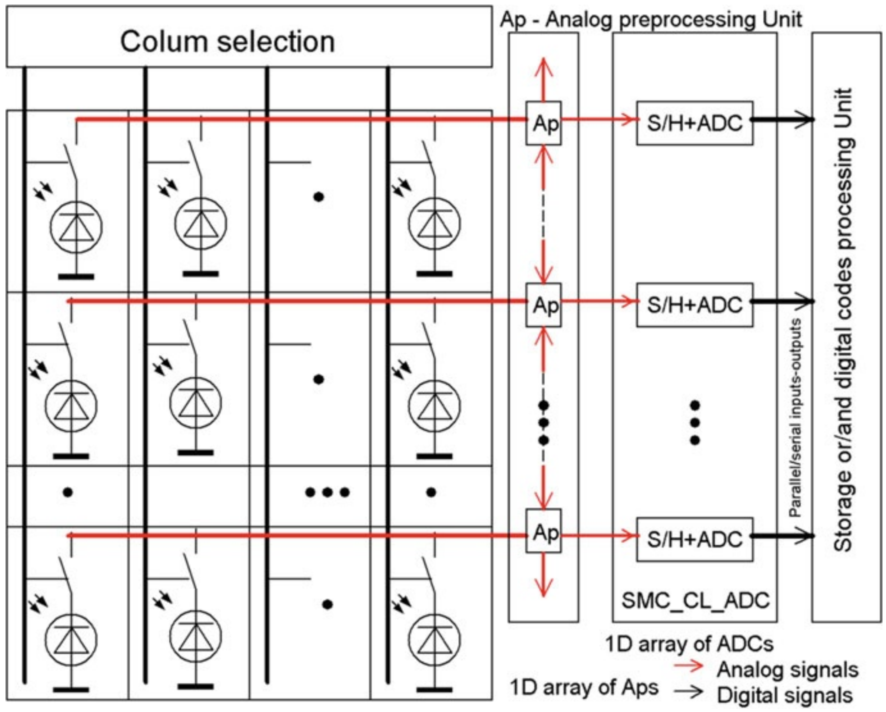
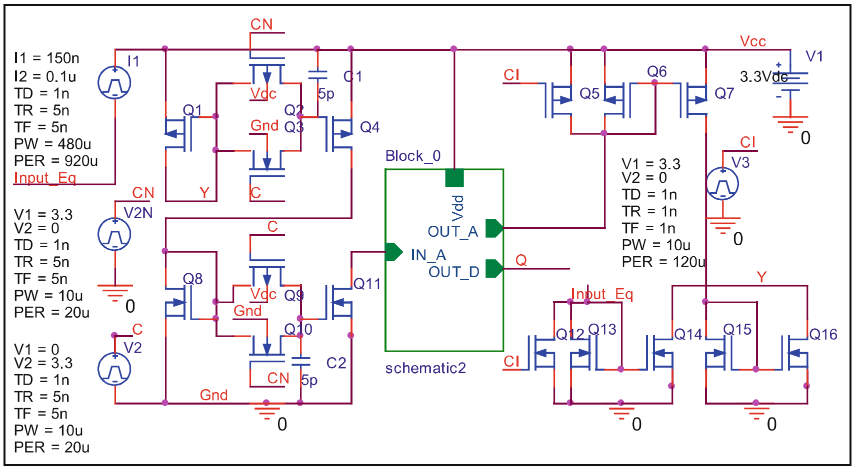


Fig. 4.19 Structure of 2D image sensor with 1D array of CL_ADC and storage or/and digital code processing unit

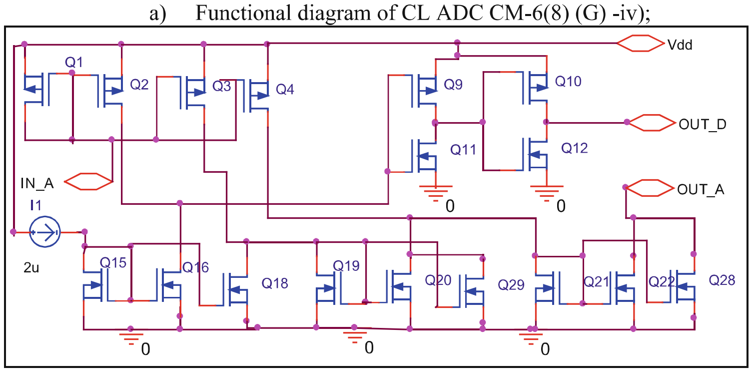
the SHD and then transmitted to the analog DC-(G), which will generate the next digital bit of the output code and the CL function.

This function is fed back to the SHD to form the next consecutive bits. The device selection and hold (SHD) consists of 18 transistors. DC-(G) consists of 15 or 17 transistors and a reference current generator. Since the circuit of one channel consists of only 33 (35) transistors, this makes it promising for multisensory systems. The DC converts the input analog signal to another output current signal, using CLF (Sect. 4.3.1) overcurrent signals and simultaneously compares it with the threshold current. The advantage of such continuous logical transformations is that the form of such transformations can be very diverse, and the operations of continuous logic used for such transformations themselves are also numerous.

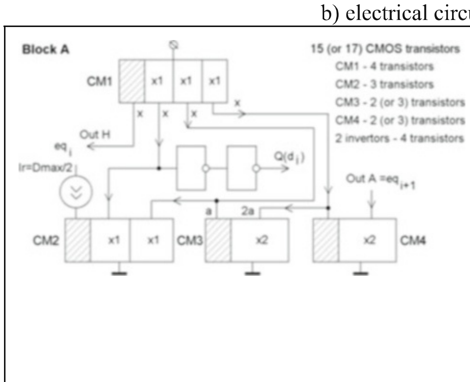
Thus, there is a wide choice for searching and optimizing such cells taking into account the required goal. To minimize the apparatus costs, cells can be very simple and consist of 10–20 transistors. In addition, the use of other known, improved dynamic and accurate indicators of current comparators [50–52], including a floating gate, etc., significantly expands the range of application of such implementations of ADC, reduces power consumption to microwatts, or significantly expands the dynamic range of input signals and maximum conversion frequencies.

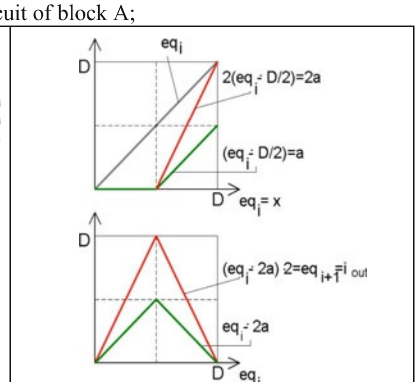


a) Functional diagram of CL ADC CM-6(8) (G) -iv);



b) electrical circuit of block A;

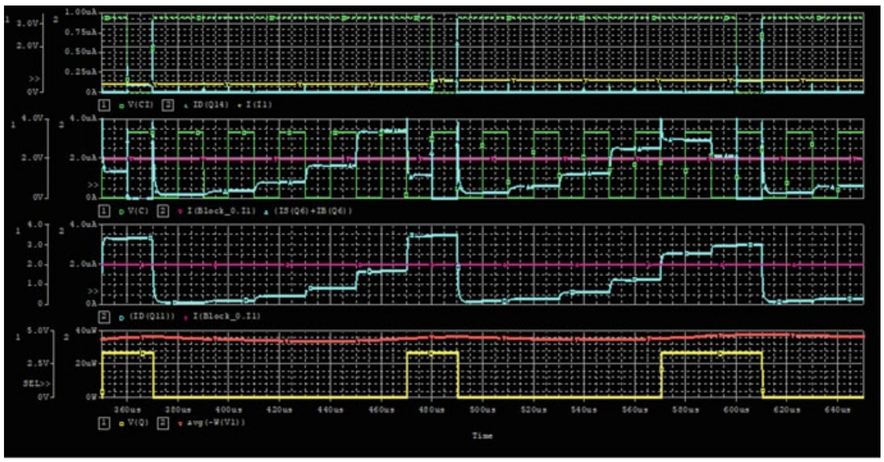




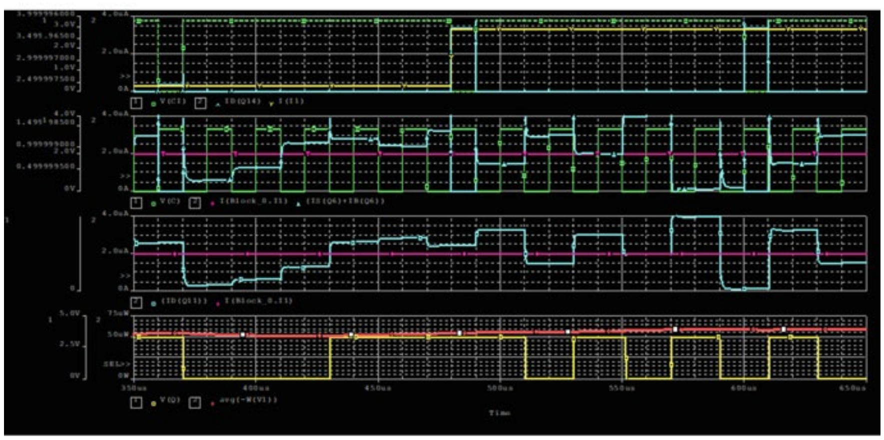
c) functional diagram of block A;	d) diagrams of continuous logical transformation of analog signal by limited difference and multiplication by 2 for realization of the equivalence function over the signal

Fig. 4.20 Circuits of the one channel of multichannel CL ADC CM-6 (8) (G)-iv with iteration transformation and base cell DC-(G). (**a**) Functional diagram of CL ADC CM-6 (8) (G)-iv. (**b**) Electrical circuit of block A. (**c**) Functional diagram of block A. (**d**) Diagrams of continuous logical transformation of analog signal by limited difference and multiplication by 2 for realization of the equivalence function over the signal

The advantage of the structure with a serial output of the Gray code is that increasing the number of iterations increases the bit ADC with an unchanged structure. To convert a serial Gray code to a binary code, only one modulo adder and one D flip-flop are required. Figures 4.21 and 4.22 show the results of simulation of one channel of six bits CL ADC CM-6 (G)-iv with iteration transformation at

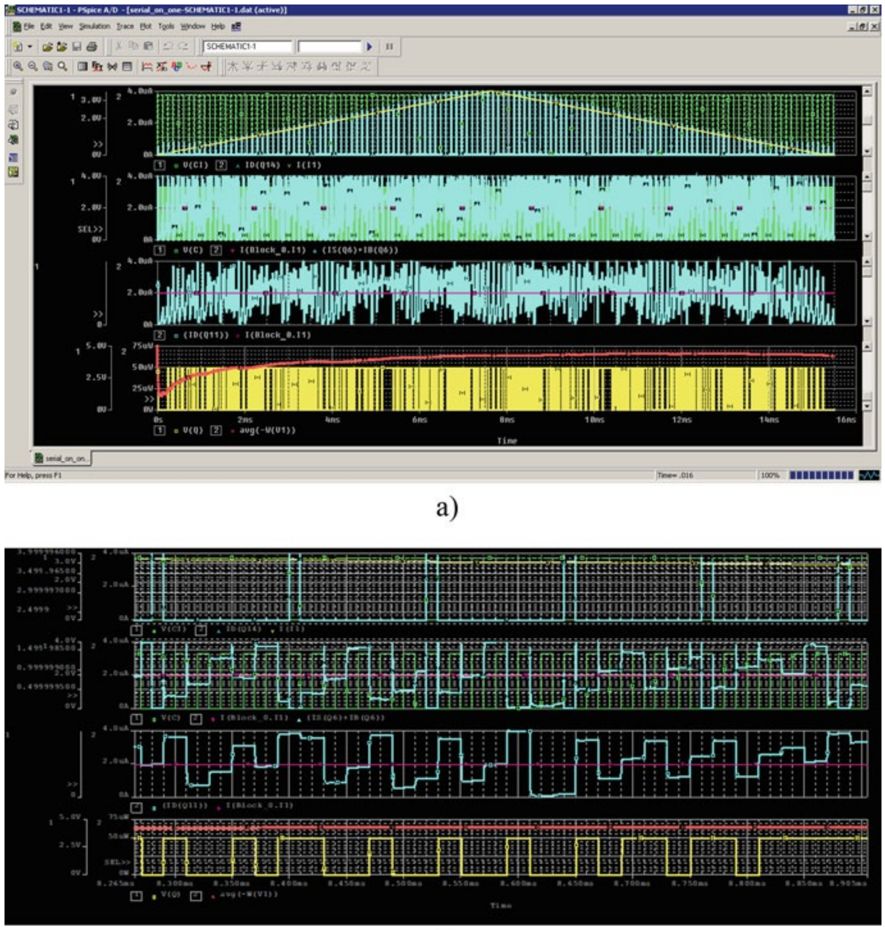


a)



b)

Fig. 4.21 (**a**) Simulation result for two input currents 100 nA and 150 nA, corresponding output Gray codes {000001} and {000011}; the blue line in the third trace is output current of the block for six-digit ADC, the violet line is the threshold current; the yellow line in the fourth trace is the output voltage of the block that corresponds to output code (a time interval for the first code 370–490 μs (six digits by 20 μs), a time interval for the second code 490–610 μs; the red line is the power consumption of about 40 μW. (**b**) Simulation result for two input currents and corresponding output Gray codes {000111} and {010101}; the consumption power is about 40 μW



a)

b)

Fig. 4.22 Simulation results of the six-digit ADC for a triangular current signal (the yellow line in the first trace): (**a**) the whole time interval; (**b**) for five time intervals with decreasing input current and corresponding output Gray code {100101}, {100100}, {100100}, {101101}, {101111} (the yellow line in the fourth trace), the red line is the power consumption of about 70 μW

linearly increasing input current signals. The total power consumption of this ADC-6 (8) (G)-iv did not exceed 70 μW with a maximum input current of 4 μA and a conversion period of 120 μS (6 × 20 μS for 6 bits) and a conversion period of 160 μS (8 × 20 μS for 8 bits). For operating modes with lower currents and Vdd = 1.5–1.8 V, the power consumption of ADC-6 (8) (G)-iv can be reduced to 10–15 μW.

The drawback of our earlier works is the lack of research on the ultimate capabilities of such structures and their precision characteristics. Therefore, in this paper, we pre-observed such a structure in the formation of eight-digit code, determined the possibility of operation with very small input currents (10 nA to 1 μA), and adding to the structure of the DAC and converters from the Gray code to the binary code (Fig. 4.23), and determined the magnitude of ADC errors and its accuracy characteristics for different modes. By reducing the requirements for high speed, the proposed diagram allows using analog-to-digital conversions for small-amplitude input currents, and the power consumption of the such single ADC channel can be less than 50 μW with Dmax = 1 μA. All the circuits are modeled on 1.5 μm CMOS transistors. Simulation of analog-to-digital conversion errors is shown in Fig. 4.24. Simulation is performed for Dmax = 4 μA, 6-bit ADC, conversion period $T = 120$ μs. Figure 4.24 shows that the maximum error is about 1 least significant bit (LSB), and only for the maximum input current, the error is about 2 LSB for the 8-bit ADC. Also, the simulation results showed that when reducing the conversion time to 10–20 μs, the errors will be the same.

In Fig. 4.23, functional diagram of CL ADC CM-(8) (G)-iv with Gray-to-binary code transformation and serial/parallel outputs with code converter and DAC for error calculation is shown. Actually the ADC itself, from which 1D or 2D arrays will be done for sensors or image processors, in contrast to the circuit in Fig. 4.20, may additionally comprise some digital elements, for example, a logic element and a trigger or register. This depends on the possible modes and requirements regarding

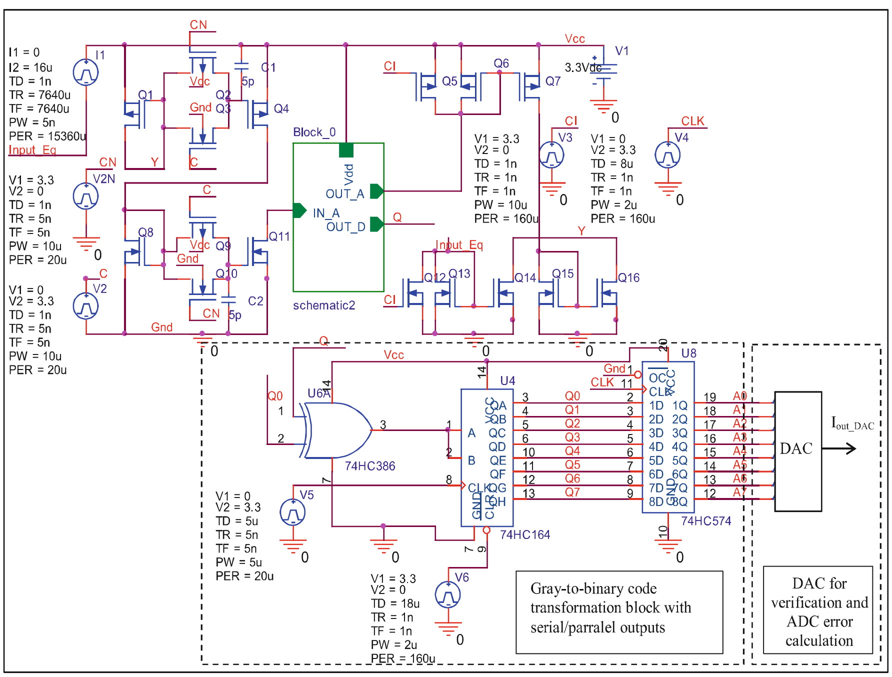


Fig. 4.23 Functional diagram of CL ADC CM-(8) (G)-iv with Gray-to-binary code transformation and serial/parallel outputs with code converter and DAC for errors calculation

the formats of output and storage of code arrays. Therefore, in Fig. 4.23, these additional optional units are marked with a dash-dotted line. To test the accuracy and timing characteristics in the dynamics, we used two registers and DAC. The results of modeling this circuit with OrCAD are partially shown in Fig. 4.24, and they confirm the correct operation and analog-to-digital and code conversion, both when linearly increasing (decreasing) and sinusoidal current signals are applied to the ADC input. They show that for the 8-bit ADC, even in high speed (Imax = 16–24 μA) and low-voltage low-frequency energy-efficient modes (with Imax = 1 μA, 4 μA), the maximum error does not exceed 4–5 quantization quanta, and the average error does not exceed 2 LSB.

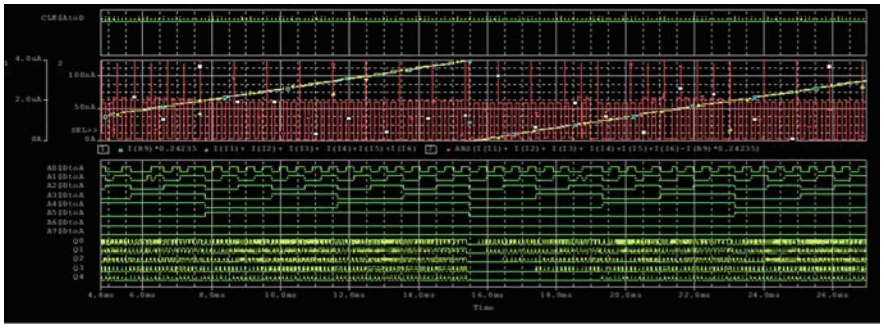
4.3.3 Simulating Parallel Conveyor CL_ADC (P_C) Based on Eight 8-DC-(G) with Parallel Serial Output

The block diagram of parallel conveyor CL_ADC (P_C) based on 8-DC-(G) (with Gray code) with a parallel serial output is shown in Fig. 4.25. The simulation results with PSpice OrCAD are shown in Fig. 4.26. Researches have shown that in such CL_ADC (P_C) 6 (8)-DC-(G) at changing Imax from 16 to 24 μA, the power consumption at 3.3 V was from 1 to 2 μW (6 bits) and 3 μW (8 bits). The conversion frequencies in the experiments were for these currents: 32, 40, and 50 MHz for 16 μA and 64 MHz for 24 μA and 40 μA.

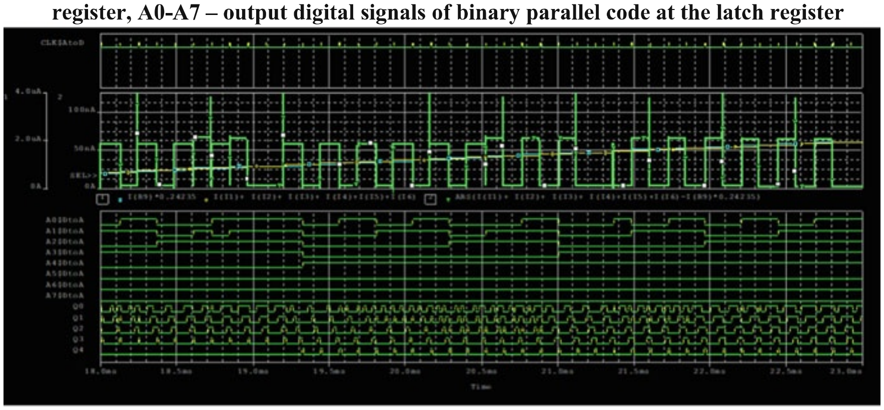
They correspond to different modes: different Imax, namely 1 μA, 4 μA, 16 μA, 24 μA, 40 μA; various 1.5 V, 1.8 V, 2.5 V, 3.3 V; various transformation periods T (0.02 μS, 0.025 μS, 1 μS, 20 μS, 100 μS), etc. These researches show that power consumption for ADC for the specified values of Imax (equal 1 μA and 1.8 V, 64 nA and 1.5 V) makes accordingly 40 μW and 2 μW, the quantization step is 15.625 nA for Imax = 4 μA and 62.5 nA for Imax = 16 μA, and quantization frequency = 40 MHz.

The essence of analog preprocessing is to find the function from the signals of several adjacent channels for different 1D and 2D windows. In this case, the 1D window is a size of 3 (may be 5, 7, 9, etc.), and the processing type is the function of finding the average of the three signals. As a function, any continuous logic functions of the type max, min, described in Sect. 4.3.1 and in paper [41], can be used.

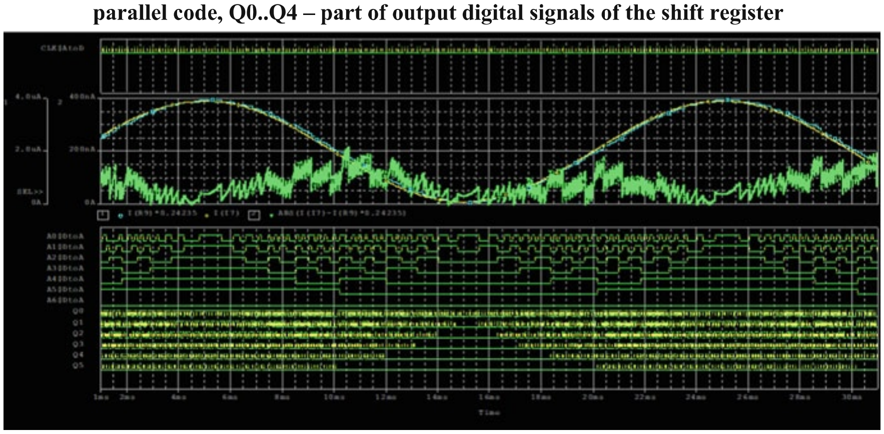
The analog preprocessing unit (Fig. 4.19) consists of 4 (6) CMOS transistors (Fig. 4.27) in this case. For functions min, max, etc., the Ap-unit consists of about 10–20 CMOS transistors. The consumption power of one-channel 8-bit ADC + Ap-unit is less than 250 μW. Simulation results of analog signal preprocessing (selecting average signal out of three neighbor channel signals) for different input signals (linearly increasing (decreasing) and sinusoidal signals) are shown in Fig. 4.28.



a) The blue line is the DAC output current, yellow line is the 8 bit ADC input current, the red line is the ADC current error (<70nA); Q0..Q7 – output digital signals of the shift register, A0-A7 – output digital signals of binary parallel code at the latch register

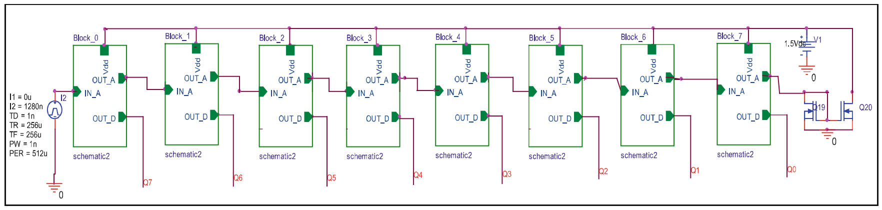


b) the blue line is the DAC output current, the yellow line is the ADC input current, the green line is the ADC current error (<70nA), A0-A7 – output digital signals of binary parallel code, Q0..Q4 – part of output digital signals of the shift register

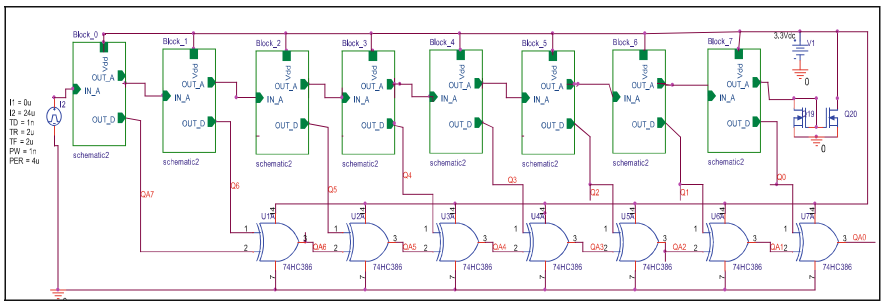


c) the blue line is the DAC output current, the yellow line is the ADC input current, the green line is the ADC current error (<200nA), A0-A6 – part outputs digital signals of 8 binary parallel code, Q0..Q5 – part of outputs 8 digital signals of the shift register

Fig. 4.24 Simulation results of the 8-bit ADC with Gray-to-binary code transformation and serial/parallel outputs. (**a**) The blue line is the DAC output current, yellow line is the 8-bit ADC



a)



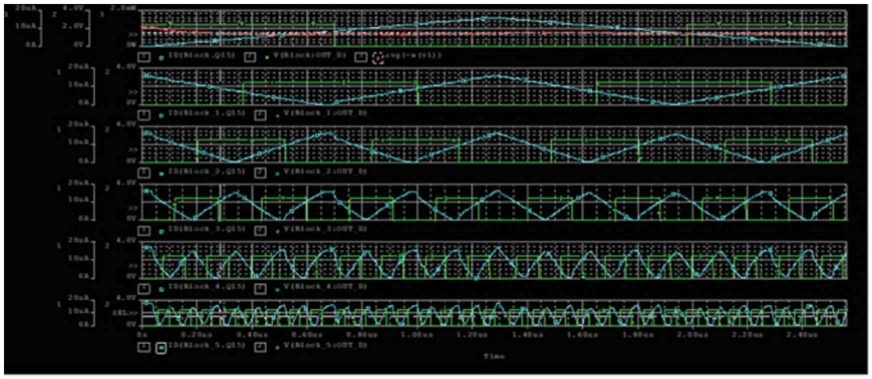
b)

Fig. 4.25 Structure of 8-bit ADC: (**a**) with Gray code parallel outputs (Q0–Q7); (**b**) with Gray-to-binary code transformation and parallel outputs (QA0–QA7)

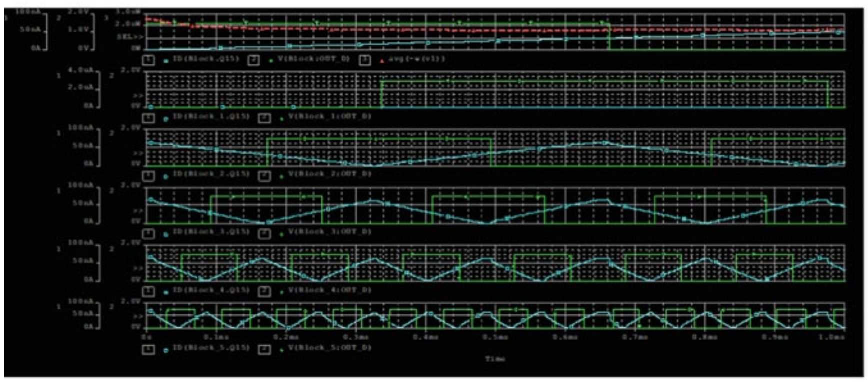
4.4 Conclusions

For the construction of mixed image processor (IP), neural networks (NNs), and image intensity transformation, the fundamentals of continuous logic cell (CLC) design based on current mirrors (CM) with functions of preliminary analog processing are proposed. Several effective schemes have been developed and modeled for CLC and optoelectronic complement dual analog neuron-equivalentors as hardware accelerators SLECNS. The proposed **CLC** have a modular hierarchical construction principle and are easily scaled. Their main characteristics were measured. They have a low supply voltage of 1.8–3.3 V, small power consumption of no more than 1 mW, processing time-conversion 0.1–1 μs, insignificant relative calculation errors (1–5%), can work in low-power modes (less than 100 μW)

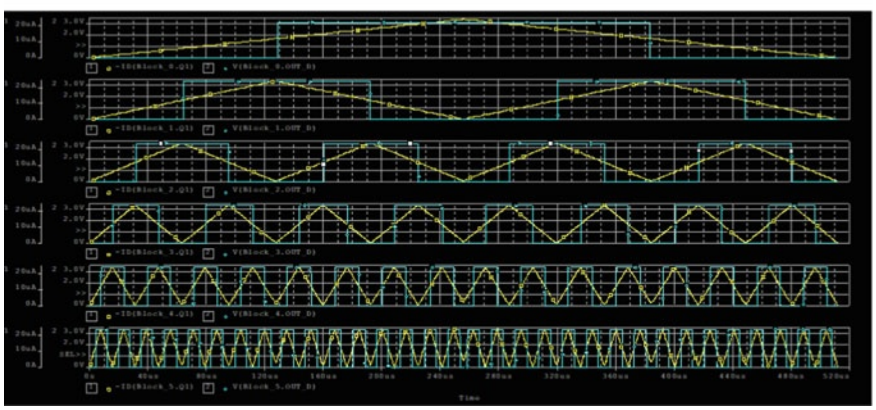
Fig. 4.24 (continued) input current, the red line is the ADC current error (<70 nA); Q0–Q7, output digital signals of the shift register; A0–A7, output digital signals of binary parallel code at the latch register. (**b**) The blue line is the DAC output current, the yellow line is the ADC input current, the green line is the ADC current error (<70 nA); A0–A7, output digital signals of binary parallel code; Q0–Q4, part of output digital signals of the shift register. (**c**) The blue line is the DAC output current, the yellow line is the ADC input current, the green line is the ADC current error (<200 nA); A0–A6, part of output digital signals of eight binary parallel code; Q0–Q5, part of output eight digital signals of the shift register



a) Time diagrams of signals of digit converting cells of 6 bit CL_ADC for mode: converting frequency F= 50MHz, input current Imax=16μA, Vdd=3.3V, consumption power P≈1mW

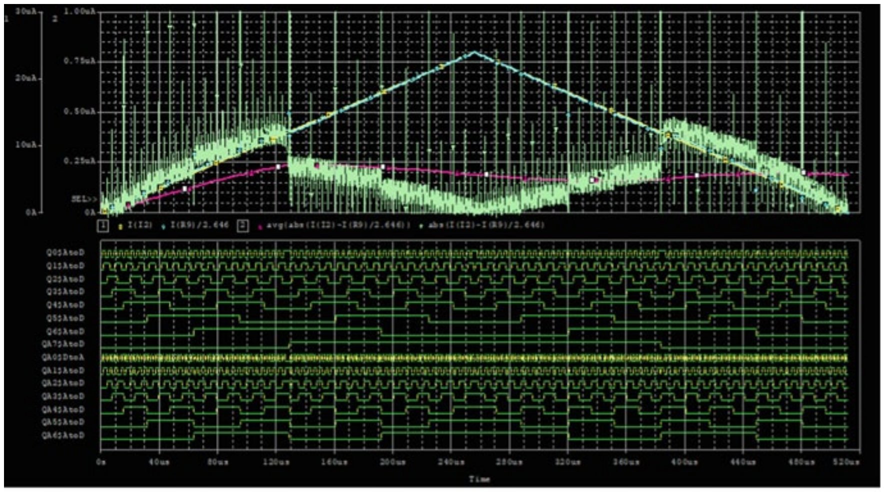


b) Time diagrams of signals of digit converting cells of 6 bit CL_ADC for mode: converting frequency F= 50kHz, input current Imax=64nA, Vdd=1.5V, consumption power P≈2μW

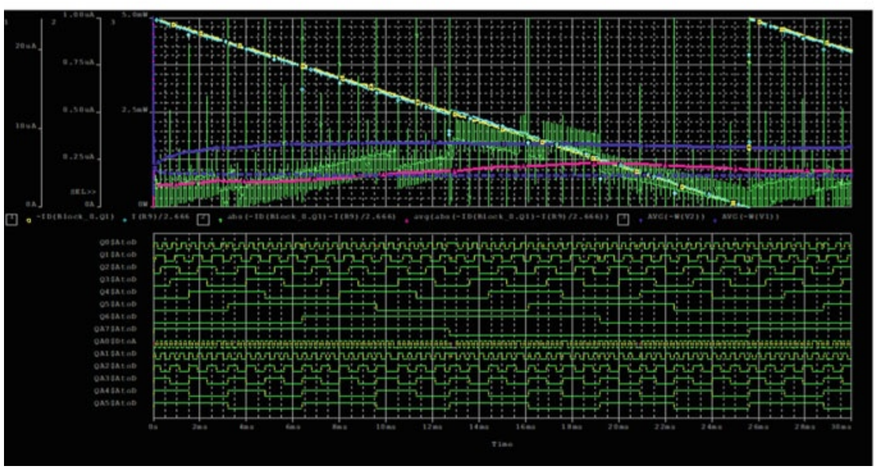


c) Time diagrams of signals of digit converting cells of 8 bit ADC (6 cells out of 8 are shown) for mode: converting frequency F= 1MHz, input current Imax=24μA, Vdd=3.3V

Fig. 4.26 Structure of multichannel 8-bit ADC (1D array 8-bit CL_ADC) and simulations results. (**a**) Time diagrams of signals of digit converting cells of 6-bit CL_ADC for mode: converting frequency $F = 50$ MHz, input current Imax $= 16\,\mu$A, Vdd $= 3.3$ V, power consumption $P \approx 1$ mW.

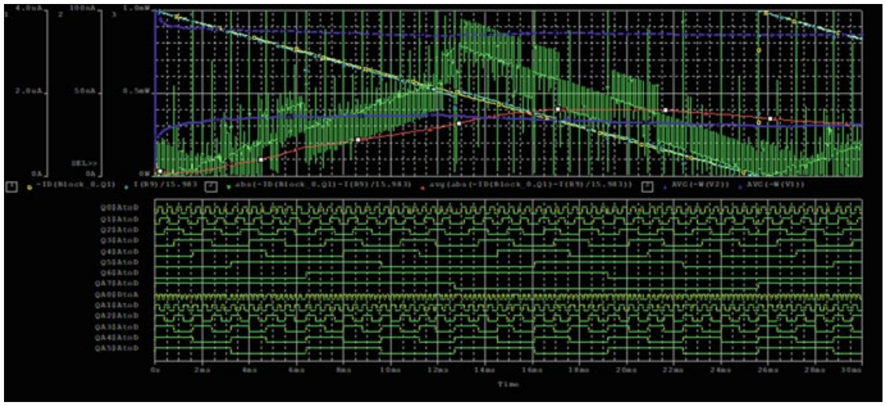


d) Time diagrams of 8 bit parallel CL_ADC signals by simulation for I_{input_max}=24µA, ADC conversion time is 1µs; the blue line is the DAC output current, the yellow line is the ADC input current, the violet line is the average ADC current error (<250nA), the green line is the ADC current error; QA0-QA7 – output digital signals of binary parallel code, Q0..Q7 (Q7=QA7) – output digital signals of Gray parallel code



e) Time diagrams of 8 bit parallel CL_ADC signals by simulation for I_{input_max}=24µA; the blue line is the DAC output current, the yellow line is the ADC input current, the violet line is the average ADC current error (<250nA), the green line is the ADC current error, the blue line is the power consumption (3mW)

Fig. 4.26 (continued) (**b**) Time diagrams of signals of digit converting cells of 6-bit CL_ADC for mode: converting frequency $F = 50$ kHz, input current Imax $= 64$ nA, Vdd $= 1.5$ V, power consumption $P \approx 2$ µW.



f) Time diagrams of 8 bit parallel CL_ADC signals by simulation for I_{input_max}=4μA, conversion frequency is 10kHz; the blue line is the DAC output current, the yellow line is the ADC input current, the violet line is the average ADC current error (<40nA), the green line is the ADC current error, the blue line is the power consumption (1.3mW)

Fig. 4.26 (continued) (**c**) Time diagrams of signals of digit converting cells of 8-bit ADC (6 cells out of 8 are shown) for mode: converting frequency $F = 1$ MHz, input current Imax = 24 μA, Vdd = 3.3 V. (**d**) Time diagrams of 8-bit parallel CL_ADC signals by simulation for $I_{\text{input\_max}} = 24$ μA, ADC conversion time is 1 μs; the blue line is the DAC output current, the yellow line is the ADC input current, the violet line is the average ADC current error (<250 nA), the green line is the ADC current error; QA0–QA7, output digital signals of binary parallel code, Q0–Q7 (Q7 = QA7), output digital signals of Gray parallel code. (**e**) Time diagrams of 8-bit parallel CL_ADC signals by simulation for $I_{\text{input\_max}} = 24$ μA; the blue line is the DAC output current, the yellow line is the ADC input current, the violet line is the average ADC current error (<250 nA), the green line is the ADC current error, the blue line is the power consumption (3 mW). (**f**) Time diagrams of 8-bit parallel CL_ADC signals by simulation for $I_{\text{input\_max}} = 4$ μA, conversion frequency is 10 kHz; the blue line is the DAC output current, the yellow line is the ADC input current, the violet line is the average ADC current error (<40 nA), the green line is the ADC current error, the blue line is the power consumption (1.3 mW)

and high-speed (1–2 MHz) modes. The relative energy efficiency of the CLC and equivalentors is estimated at a value of not less than 10^{12} an. op./sec. per watt and can be increased by an order. The correctness of the chosen concept is confirmed by the obtained results of the design and creation of neuron equivalentors (**NEq**s) and MIMO structures based on them. Such neuron equivalentors can form the basis of promising self-learning biologically inspired devices SLECNS and CNN, in which the number of such parallel-running **NEq**s is 1000. Thus, we have proposed implementation options for digital-analog cells (DC) and CL structures of the ADC CM. Such ADCs are simple, and only one DC is required for the iteration type, supplemented by a sample and hold device. The advantage of the ADC is the ability to easily implement parallel code, as well as serial parallel output code. Results of circuit simulation using OrCAD are shown. Such simple structure of CL ADC CM with low power consumption ≤3 mW and supply voltage 1.8–3.3 V, and at the same time with good dynamic characteristics (frequency of digitization even for 1.5 μm

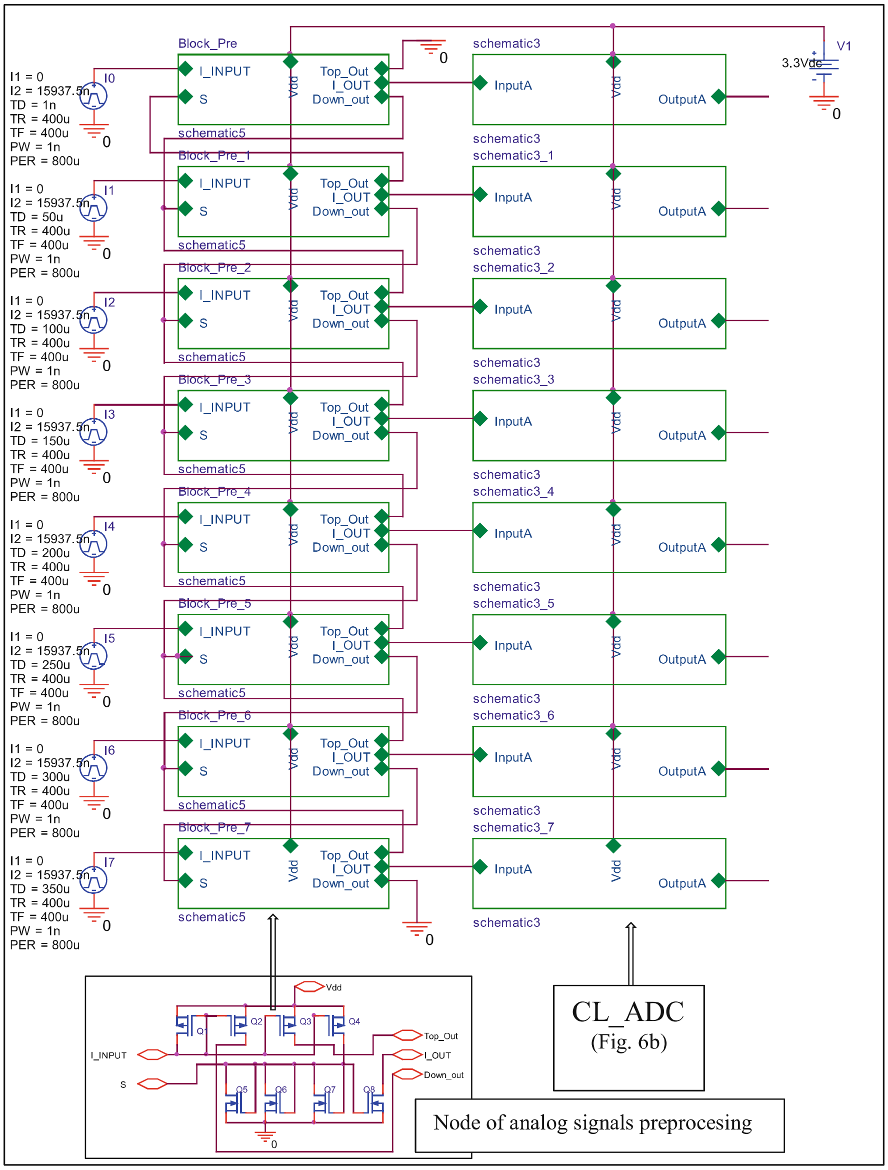
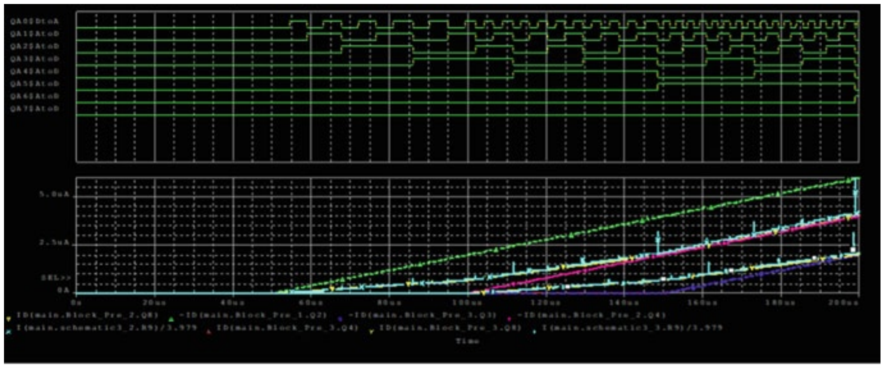
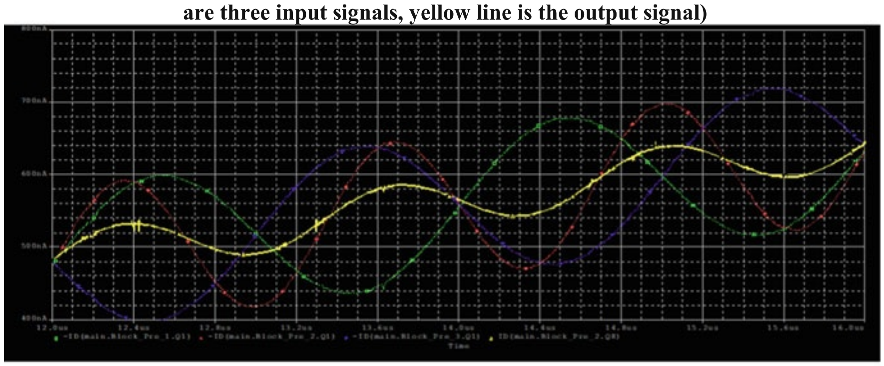


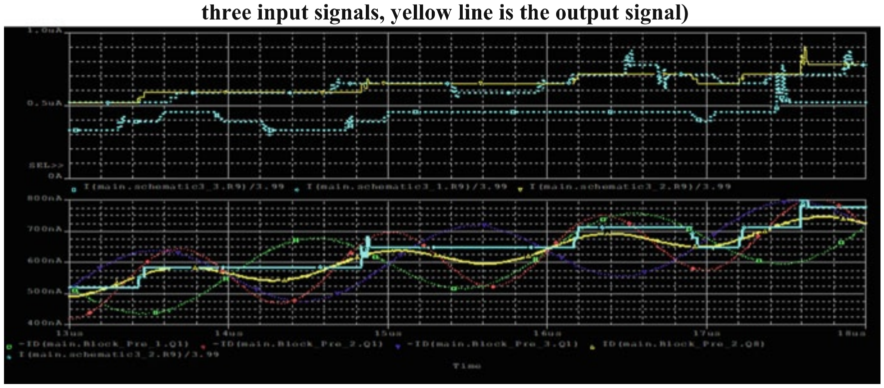
Fig. 4.27 Structure of multichannel 8-bit ADC (1D array 8-bit CL_ADC) with analog signal preprocessing



a) simulation results of analog signals preprocessing (selecting average signal out of three neighbor channels signals): green, blue, violet lines are three input signals, yellow line is the output signal)



b) simulation results of analog signals preprocessing (selecting average signal out of three neighbor channels signals): green, blue, red lines are three input signals, yellow line is the output signal)



c) simulation results of analog signals preprocessing (selecting average signal out of three neighbor channels signals): green, blue, violet lines are three input signals, yellow line is the output signal), light blue is the DAC output signal

Fig. 4.28 Structure of multichannel 8-bit ADC (1D array 8-bit CL_ADC) with analog signal preprocessing. (**a**) Simulation results of analog signal preprocessing (selecting average signal

CMOS-technologies is 40 MHz, and can be increased up to ten times) and accuracy (Δ quantization = 15.6–62.5 nA for Imax = 4–16 μA) characteristics are shown. Taking into account the sensitivity of modern photodetectors, the range of optical signals can be 1–200 μW. For the ADC of iteration type, one channel consists of one DC-(G) and SHD, and it has only 35–40 CMOS transistors. Thus, such 1D and 2D arrays of successive ADCs are very promising for sensors and IP. The general power consumption of one ADC, in this case, is only 50–70 μW, if the maximum input current is 4 μA. For high performance and frequency of conversions, it is preferable to use the parallel pipeline CL_ADC (P_C) scheme based on the set of 8-DC-(G) with parallel serial outputs. The maximal error is about 1 LSB, and only about 2 LSB for 8-bit CL ADC for the maximal input current. CL ADC CM with analog signal preprocessing opens new prospects for realization linear and matrix (with picture operands) micro photo-electronic structures which are necessary for neural networks, digital optoelectronic processors, neuro fuzzy controllers.

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Fig. 4.28 (continued) output of three neighbor channel signals): green, blue, violet lines are three input signals, yellow line is the output signal. (**b**) Simulation results of analog signals preprocessing (selecting average signal output of three neighbor channels signals): green, blue, red lines are three input signals, yellow line is the output signal. (**c**) Simulation results of analog signal preprocessing (selecting average signal output of three neighbor channel signals): green, blue, violet lines are three input signals, yellow line is the output signal, light blue is the DAC output signal

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