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ABSTRACT

The method of resolving power enhancement of analog-digital conversion path of jitter analyzers in fiber-optical networks is suggested in the research. The analog-digital path is designed on the basis of the principle of phase-plane correction of dynamic errors and is characterized by high resolving power.

Keywords: jitter, analog-digital conversion path, fiber-optical networks, phase-plane correction.

1. INTRODUCTION

Some specific problems appear in modern fiber-optical networks. These problems are connected with the transmission peculiarities of digital signals to paths of telecommunication means. Phase jitter (PJ) is one of the main problems, which appears during the design, production and operation of modern digital telecommunication networks. PJ is a specific type of distortions, which appear in the process of formation and transmission of signals in paths of fiber-optical networks[1].
In the conditions of the modern development of digital telecommunication means, the problem of PJ signals in fiber-optical networks becomes a particular urgency, because as a result of the introduction of new methods of transmission involving higher data transmission speeds, signals jitter causes the appearance of bit errors, as well as uncontrolled synchronization slippage and errors. This, in turn, leads to a significant decrease in the functioning stability of telecommunication means, the deterioration of the communication quality, and sometimes loss of communication[2]. Therefore, when developing and operating telecommunication means, one of the most important quality indicators is the value of PJ signals in fiber-optical networks.

In order to guarantee the appropriate quality of communication signals, the PJ is measured at the output of each network interface, as well as PJ of each digital equipment or digital section of the transmission system. At the same time, the development of new digital telecommunication technologies puts forward requirements for increasing the efficiency of PJ signals estimation in fiber-optical networks.

The main factor determining the effectiveness of PJ estimation is the quality of the jitter signal processing itself. Parameters of jitter can acquire values that are in a wide dynamic range. Therefore, the main requirement put forward to the jitter analyzer is the low level of its own PJ. Modern jitter analyzers are characterized by their own PJ, which has a value of 0,05 unit intervals (UI) and above. Such values of the self PJ do not allow to analyze the jitter of FOTS with the resolving power according to the main parameter at 0,01 UI[2].

2. PUBLICATIONS ANALYSIS

The current level of PJ analyzers does not allow to create jitter estimation devices with their own PJ approaching 0 UI, therefore, the own jitter of the analyzer always affects the final results of the analysis of the quality of fiber-optical networks[3].

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One of the main stages of processing the jitter signal formed at the output of the phase detector is its analog-digital conversion[3]. It is the components of the analog-digital conversion path (ADCP) that determine the characteristics of the jitter estimation device as a whole[4].

Despite a number of issues already solved, with the use of analog-digital converters (ADCs) in jitter estimation devices, there are still many problems that hamper the widespread use of ADCs in jitter analyzers of fiber-optical networks. Namely: low resolving power in the high-frequency range of input signals (from 10 MHz and above), insufficiently developed methods of analog-digital conversion with correction of dynamic errors, which causes the restriction of the efficient capacity of the ADCP of jitter analyzers[5].

These problems are related both to the lack of the necessary element base, and the complexity of the processes of analog-digital conversion of variables in time of high-frequency signals, the mathematical description of which in the time and frequency measurement is rather complicated. Thus, modern circuitry does not provide the realization of the potential of high-speed ADCs, which limits the efficiency of the use of jitter analyzers in fiber-optical networks[5].
The task of developing ADCs is far from completion that provide high resolving power when converting jitter signals, which are characterized by a wide spectrum and are noisy. The consequence of this is the discrepancy between the dynamic parameters of serially produced ADC chips and the set criteria that are necessary to fulfill the conditions for the effective functioning of the ADCP in the fiber-optical networks[6, 8, 9].

On the basis of the above-stated statements, the actual task is to develop a method for increasing the resolving power of an analog-digital conversion path with the correction of dynamic errors, which will allow to carry out the transformation of signals in a wide frequency band and is characterized by high resolving power and the correspondence of conversion errors to the declared resolving power of jitter analyzers in fiber-optical networks[10, 11, 12].

3. RESEARCH OBJECTIVES AND TASKS

The aim of the work is to increase the resolving power of the analog-digital converter path of jitter analyzers in fiber-optical networks by adjusting dynamic errors. To achieve a given goal, the following tasks need to be solved:

- to work out the correction method of dynamic errors of the ADCP in the phase plane;
- analyze the effectiveness of the ADCP with the correction of dynamic errors;
- to develop the structure of the ADCP of jitter signals.

4. BASIC RESEARCH MATERIAL

The most effective way to reduce the dynamic errors of ADC is the methodology for monitoring and correction of the process of analog-digital conversion. The essence of this methodology is that, at given moments of time, the control of the process of an analog-digital conversion and, if necessary, the correction of the conversion process towards the reduction of dynamic errors are performed [7, 11, 12].

The method of controlling the dynamic properties of the ADC should be based on the model of the research object - ADC. According to the metrological model of the ADC, the study of dynamic properties is to determine the dynamic errors by sending a test signal and pulses of discretization, recording and processing of the results of analog-digital conversion [7, 13, 14].

The dynamic error of the ADC in the i - step can be represented as the difference between the output signal of the ADC and the digital equivalent of the ideal quantized input signal without taking into account static errors

$$\Delta_d(i \cdot T_S) = y(i \cdot T_S) - x(i \cdot T_S), \quad (1)$$

where $y(i \cdot T_S)$ – the output signal of ADC, $x(i \cdot T_S)$ – the ideal quantized input signal of ADC, T_S – discretization period.
The accuracy of determining the dynamic characteristics according to the method of the "black box" is significantly influenced by static errors of the ADC. To overcome this factor, the following rules must be followed.
1. ADC monitoring in a dynamic mode can be performed only after the its static properties for compliance with the set

standards are pre-checked [15,16,17].

2. In dynamic research, the ADC should function in such a mode, in which the dynamic error of the conversion significantly exceeds the static ones. This is necessary for a reliable estimation of ADC dynamic characteristics if the errors found are a general manifestation of the dynamic and static ADC properties. If necessary, the non-ideality of static ADC parameters can be taken into account at the stage of processing of the measurement results.

For the ADC input signal $U(t)$ the dynamic distortions are proportional to the signal change rate

$$\Delta_d(i) = \left(\left. \frac{dU}{dt} \right|_{t=t_i} \right) \cdot \tau_{d_i} . \tag{2}$$

In this regard, instead of the set of input signals, one can consider the phase space of a trajectory of a system generating input signals $U(t)$. Then, a given class of input signals of this type of ADC corresponds to a certain region in the phase plane $\{U, dU/dt\}$. The choice of a test signal is to select a trajectory in this plane [18, 19, 20].

One of the directions of the implementation of the correction process, taking into account the speed of the change of signals, is the use of the correction table of space-state (TSS) (fig. 1).

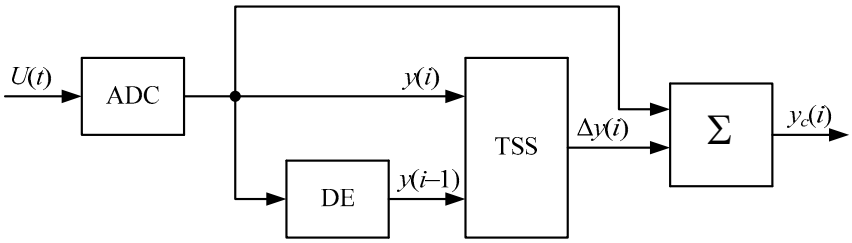

Figure 1. The general structure of the process of adjusting the dynamic errors of the ADC on the basis of TSS

In this case, the current value of the ADC $y(i)$ and the previous value $y(i-1)$ form the address due to which the output value of ADC is found

$$\left[y(i-1), y(i) \right] \to \Delta y(i) . \tag{3}$$

At the same time n- bit samples $y(i)$ and $y(i-1)$ are combined to form an address in TSS with the capacity of $m = 2 \cdot n$. This addressing creates a two-dimensional overview table, where $y(i)$ and $y(i-1)$ are used to form these two dimensions.

For synchronous receipt of the previous value $y(i-1)$ a delay element (DE) is used.

A two-dimensional table is the simplest implementation of the space-state method. In the general case, l delayed samples can be used to form the address of the correction coefficient:

$$\left[y(i), y(i-1), ..., y(i-l) \right] \to \Delta y(i) . \tag{4}$$

In this case, there are l elements of delay that synchronize the formation of the combined address by bit $m = (l+1) \cdot n$. Obviously, for such a method, there is a problem of increasing the amount of memory to store correction coefficients $M = 2^m = 2^{(l+1) \cdot n}$. Therefore, the use of TSS is only possible to correct the dynamic errors of low-level ADCs of low speed.

An effective way of reducing the dynamic ADC errors is to adjust the results of the analog-digital signal transformation in the phase plane [7].

It is necessary to pre-determine the error $\Delta_d(i \cdot T_S)$ for each i - quantized value of the output signal of the ADC. The

error at each step of quantization depends not only on the inertial properties of magnitude of the dynamic the ADC, but also on the change rate of the input signal at the input of the converter. Therefore, when determining the dynamic error $\Delta_d(i \cdot T_S)$, it is expedient to take into account the source code of the ADC $y(i \cdot T_S)$ and the steepness of the signal $y'(i \cdot T_S)$. That is, it is possible to obtain an estimate of the dynamic error as a function of two variables $\Delta_d[y(i \cdot T_S), y'(i \cdot T_S)]$.

The generalized structure of the adjustment process based on the phase plane is presented in fig. 2.

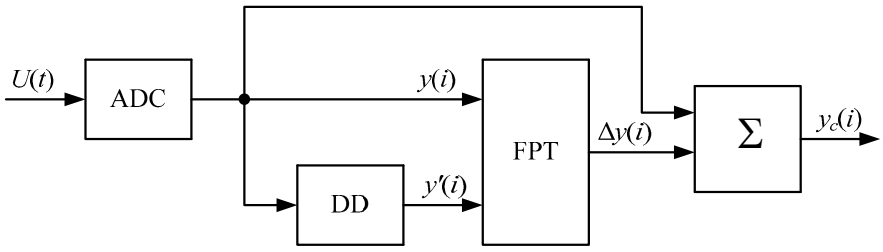

Figure 2. Generalized structure of the process of phase-plane correction of dynamic ADC errors

Phase-plane addressing in this structure is an alternative to the previous address of space of states. In this case, a two-dimensional phase-plane table (FPT) is used, in which the correction members are stored. The addresses for such a table are formed from the current sample of ADC $y(i)$ and the estimation of the steepness of the signal for each sample $y'(i)$:

$$\left[y(i), y'(i)\right] \rightarrow \Delta y(i). \tag{5}$$

In general, the signal strength can be determined using a digital differentiator (DD).

The adjustment of the results of analog-digital conversion in the i - step is performed by subtracting from the output value of the ADC the received estimate of the dynamic error. Then the adjusted ADC value can be written as

$$y_c(i \cdot T_S) = y(i \cdot T_S) - \Delta y[y(i \cdot T_S), y'(i \cdot T_S)]. \tag{6}$$

Using the phase-plane method of resolving power enhancement leads to an increase in the volume of components and nodes of the ADCP, most of all its digital part, and to an increase in the conversion time, due to the need to perform additional operations to process the results of analog-digital conversion. However, this disadvantage is weakened by the simplification of the analog part of the device and the fundamental ability to build accurate analog-digital conversion devices on inaccurate digital nodes.

In the study of the dynamic properties of ADCPs, the problem of selecting test signals must first be solved. To calculate the values $\Delta y[y(i \cdot T_S), y'(i \cdot T_S)]$, it is necessary to select the type of test ADC input signal that allows the calibration of all quantified ADC levels and to investigate the adequacy of the ADC dynamic error estimates.

To calibrate ADCP as test influences are most often used: stepwise, pseudorandom and harmonic signals. One-signal calibration technique is based on the mechanism of accumulation of distortions of the sinusoidal test signal of ADCP. But the ADCP in jitter analyzers functions with multi-frequency signals, with the transformation of which, in addition to the constituents of the main and harmonic frequencies, there are intermodulation distortions and noise components. Therefore, the estimates of the dynamic error found by the one-signal method are reliable only in the case of ADCP with sinusoidal signals.

The nonlinearity of the conversion of the ADC leads to a violation of the principle of superposition, and therefore the corrected values of the analog-digital transformation when working with harmonically saturated signals by the result of calibration on single-frequency signals are incorrect [6]. Proceeding from this, the optimal test signal that creates the conditions for detecting the nonlinearity of the ADC that results in harmonic and combined signal distortion is a biharmonic or dual-tone signal whose spectrum contains two harmonic components with frequencies ω_1 and ω_2 and amplitudes U_{m1} and U_{m2}:

$$U_T(t) = U_{m1} \cdot \cos \omega_1 t + U_{m2} \cdot \cos \omega_2 t \,. \tag{7}$$

The Hilbert transform can be used to investigate the behavior of a two-tone overturning signal

$$U_B(t) = \left[U_T^2 + \hat{U}_T^{*2}(t) \right]^{1/2}, \tag{8}$$

where $\hat{U}_T^*(t)$ – the signal connected to the original.
For a given two-tone signal $U_T(t)$, the connected signal

$$\hat{U}_T^*(t) = U_{m1} \sin(\omega_1 t) + U_{m2} \sin(\omega_2 t) \,. \tag{9}$$

Instantaneous signal frequency

$$\omega(t) = \frac{U_T'(t) \cdot \hat{U}_T^*(t) - U_T^{*'}(t) \cdot U_T(t)}{U_T^2(t) + \hat{U}_T^{*2}(t)} \,. \tag{10}$$

Substituting the values $U_T(t)$ and $\hat{U}_T^*(t)$ in (9) and (10) and taking into account that $U_{m1} = U_{m2}$ and $\omega_2 - \omega_1 = \Delta\omega$, it is possible to gain

$$U_B(t) = U_{m1} \left[2 + 2\cos(\Delta\omega \cdot t) \right]^{1/2}. \tag{11}$$

Taking into account (7) and (8) the final expression for the two-tone test ADC signal will look like

$$U_T(t) = U_{ADC} \cos(\Delta\omega \cdot t) \cdot \cos\left[(\omega_1 + 0{,}5\Delta\omega) \cdot t \right], \tag{12}$$

where $U_{ADC} = 2U_{m1} = 2U_{m2}$ – the maximum voltage of the input signal of the ADC, which sets the condition of coverage by the test effect of the full dynamic range of ADC [21].
A two-tone signal forms a beat with the frequency of $\Delta\omega$. The total signal-beat is not sinusoidal, although it looks similar to it. Thus, the selected two-tone test signal allows for the harmonic and combinative distortion correction of the analog-digital transformation to be taken into account, using historically established methods for investigating nonlinear devices. At the same time, two-frequency oscillations are easy to implement with existing certified sine wave generator or frequency synthesizers [24].

Now, it is necessary to find out how the two-tone test signals are adequate to the task of determining the correction coefficients on the set of input signals of the ADC. One of the ways of describing physical processes is their description in a phase plane. If the signal can be described by coordinates x and y, then for the analysis of signal parameters it can be represented in a rectangular coordinate system, which in this case is called phase coordinates. There is no timestamp t in explicit form on this image. Indirectly, the time is given in the following way: for each time point t_i corresponds a fixed coordinate value $x(t_i)$ and $y(t_i)$, which is displayed in the axes x and y point. When t is changed, the image point is moved by the phase plane, leaving a trace called the phase trajectory. The ADC input signals must satisfy the conditions

$$\begin{aligned} &-U_{ADC} < U_T(t) < U_{ADC}; \\ &-S < \frac{dU_T(t)}{dt} < S, \end{aligned} \tag{13}$$

where $-S$ and S – the limiting values of the steepness of the signal on the input of the ADC.
The phase portrait of the two-tone signal taking into account (12) is shown in fig. 3.

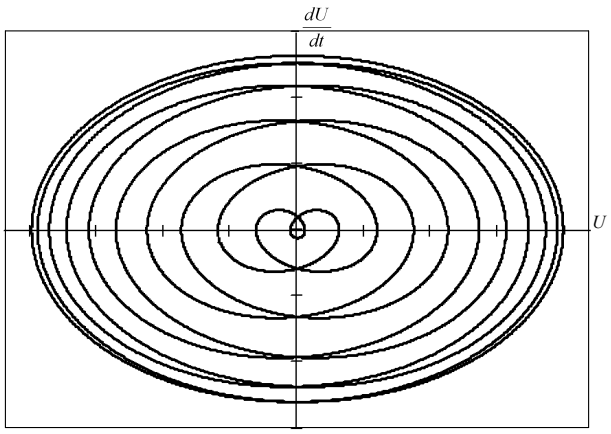

Figure 3. Two-tone test signal in the phase plane

As it can be seen from this figure, the phase trajectory of the investigated signal on the phase plane is limited to a rectangle with vertices U_{ADC}, $-S$, $-U_{ADC}$, S. Dynamic error of ADC is determined at points located on the phase trajectory. By changing the frequency or amplitude of the test signal, the given phase plane can be overlapped with control points. At the same time, combining the pair of coordinates $(x;\ dx/dt)$ it is possible to obtain the set of given speed of signal change and its level in any part of the phase plane, which corresponds to the probable values of the real ADC signal.

The test signal $U_T(t)$ as a function of time must satisfy the general requirements for the input signals of the ADC. First, the values $U_T(t)$ and $U_T(t)/dt$ at any time must match the region of the phase plane $\{x,\ dx/dt\}$, which is determined by the admissible set of input signals of the converter. Secondly, the choice of the frequency band of the test signal must satisfy the conditions of the theorem of Kotelnikov-Nyquist, because the failure to fulfill these conditions will lead to additional errors of the spectra overlaying. So, the sampling frequency of the ADC

$$\omega_S > 2\omega_2 . \tag{14}$$

In addition, the two-tone signal has an appropriate bandwidth, so an additional frequencies ω_1 and ω_2 setting condition can be written as

$$\omega_2 - \omega_1 << 0,5(\omega_2 + \omega_1) . \tag{15}$$

Based on the last expression, it can be argued that components of the biharmonic signal should have frequencies that differ by values not bigger than 10 %.

The development of the phase-plane correction method has put forward the requirements for providing high resolving power of ADCP, which is represented by an effective amount of bits. The expression for an effective number of ADCP bits with known quantization noise has the form [5]

$$n_{ef} = \frac{\log_2 10}{20} S/N + \log_2 \frac{U_{ADC\,m}}{\sqrt{6}\cdot U}, \tag{16}$$

where $U_{ADC\,m}$ – the maximum value of the input signal of ADC.

If the value of the input signal $U = 10^{-\frac{U_{in}}{20}} \cdot 0,5U_{ADC\,m}$, then taking into account (16) we obtain

$$n_{ef} = n - 0,5 \cdot \log_2 \left(1 + 3\frac{\delta_D^2}{h^2} + a_\tau^2 \cdot 2^{-m} \right). \tag{17}$$

We introduce in expression (17) the corrective component of the method. Under the condition (6), the dynamic error is compensated to a given level. Then the effective number of ADCP bits with correction in the phase-plane region, taking into account the number of correction members, is:

$$n_{ef\,c} = n - 0,5\log_2\left(1 + 3\frac{\left(\delta_D - \Delta y\right)^2}{h^2} + a_\tau^2 \cdot 2^{-m}\right). \tag{18}$$

On the basis of the information theory and the results of the optimal adjustment, we can find the limit values of the mean square error of the ADCP for a given input signal class. Hence, the effective number of bits is equal to:

$$n_{ef\,c} = n - 0,5\log_2\left(1 + 10^{\frac{U_{in}}{10}} + 2^{-m}\right). \tag{19}$$

In this expression, for an effective bit ADC with correction, there is no component of the dynamic error in the explicit form, although it indirectly influences the level of the input signal. The obtained expression allows to construct graphs of dependencies of the effective number of digits of the basic ADCP and an analog-digital conversion device with correction from the value of the input signal (fig. 4).

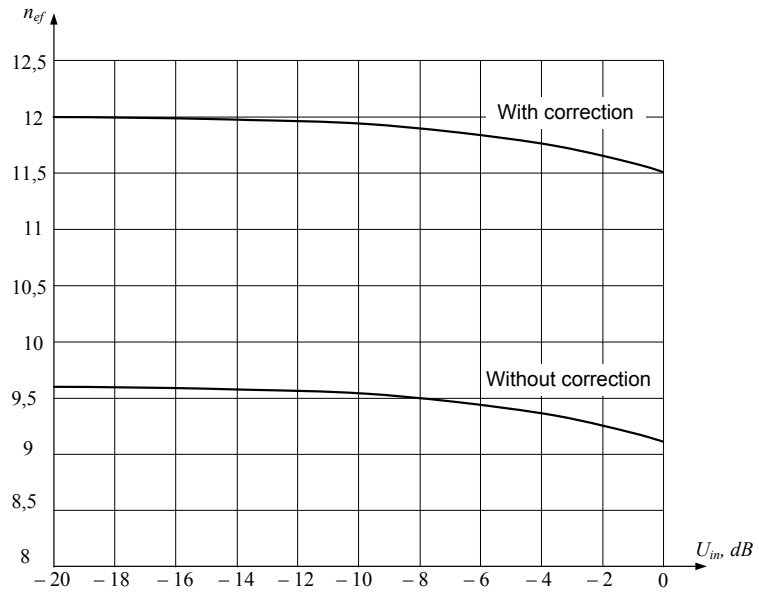

Figure 4. Dependence of the effective number of bits of ADCP on the level of the input signal

5. PRACTICAL RESULTS

From the figure it can be seen that in the range of changes in the input signal levels of the base ADC -20 ÷ -10 dB, the effective number of bits decreases insignificantly. The main reduction of the effective ADCP bit rate is observed in the range of -20 ÷ 0 dB, which is explained by the "coverage" of the whole scale of analog-digital conversion at high values of the input signal. In this case, the base ADC without correction shows a decrease in resolving power of 2,4 bits compared with the correction mode over the entire range of input signal.

The implementation of the method of phase-plane correction of dynamic errors of ADCP was carried out on the basis of the generalized structure of the correction process. The structure of the analog-digital conversion path of jitter signals is presented in fig. 5.

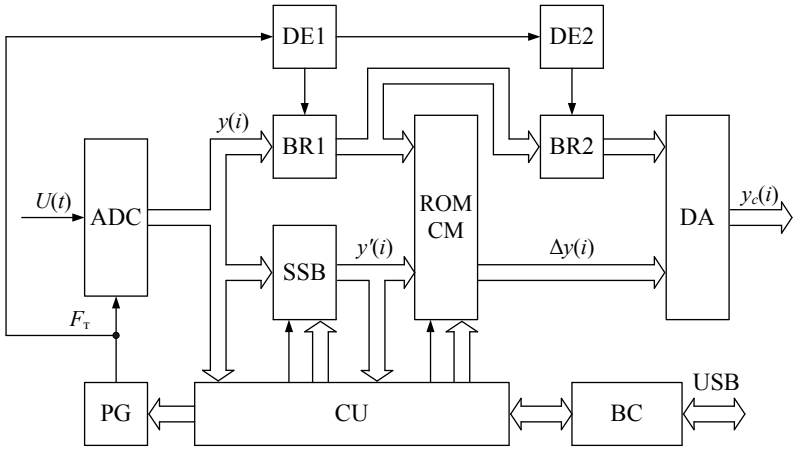

Figure 5. The structure of the analog-digital conversion path of jitter signals with errors correction

The device contains an input bus $U(t)$, a clock bus $F_т$, an output bus $y_c(i)$, USB bus, a base ADC, buffer registers (BR1, BR2), an input signal steepness block (SSB), ROM of correction members (ROM CM), a digital adder (DA), delay elements (DE1, DE2), pulse generator (PG), USB bus controller (BC) and control unit (CU). The analog-digital conversion unit operates in two modes. In the calibration mode, the biharmonic test signal $U_{DT}(t)$ is sent to the input bus. In this mode, an analog-digital conversion device connects via a USB bus to a computer.

In the first step of calibration, the parameters of the test signal are entered: U_m, f_1, f_2, the value of the sampling rate F_s and the bit rate of the ADC *n*. Then the calculation of the sample size *M* and the number of correction members *m* are performed. Further on the control signal from the CU, the PG starts with quartz frequency stabilization $F_т$.

The digital equivalents of the input ADCP signal $y(i)$ and the digital signal of the steepness of the input ADCP $y'(i)$ through the CU and BC are sent into the computer's RAM memory (RAM). After the accumulation of a given input data array $\left[y(i);\, y'(i)\right]$, the correction members $\Delta y(i)$ are calculated and the phase-plane table of correction coefficients is formed. This array via the USB, BC, and CU bus is recorded in the ROM CM.

In working mode, the analog-digital conversion path is disconnected from the computer and the real analog signal is sent to the input bus of the converter. The ADC source code is sent to BR1 and SSB. In BR1, the digital countdown of the signal is stored for the delay time in the SSB. This is necessary for the simultaneous receipt of signals to both ROM CM address inputs. Output codes BR1 and SSB form the address of the correction member sample $\Delta y\left[y(iT_s);y'(iT_s)\right]$, namely, the output signal BR1 creates the first part of the address of the cell of the correction member $\Delta y(iT_s)$, and the output signal of the SSB is the second part of the address of the corrective member. Additionally, the BR1 output signal is sent to the BR2 input, which stores it at the time of the sampling of the correction member from the ROM CM.

At the last transformation, the output signal BR2 enters the first DA input, and the correction term is applied to the second input of the DA from the output of the ROM CM. The corrected result of the analog-digital conversion is formed at the output of the DA: $\Delta y_c(iT_s) = y(iT_s) - \Delta y\left[y(iT_s);y'(iT_s)\right]$.

To reduce the effect of reducing the speed of an analog-digital conversion with correction blocks, the device operates in conveyor mode. With the conveyor organization of analog-digital conversion, regardless of the number of cascades, that is, the successive stages of conversion, the full conversion time is equal to only one tact.

6. CONCLUSIONS

The analog-digital conversion path PJ signals is the key to jitter estimation in fiber-optical networks, as the main dynamic parameters of the ADCP directly affect the efficiency of the functioning of the estimation means of the PJ.

The method of correction of dynamic errors of an analog-digital conversion path is suggested, which is based on the formation of correction members in the phase plane, which allows to take into account not only the current values of the source code of the basic ADC but also its steepness. Based on the analysis of the effective ADCP bit rate, it is shown that the phase-plane correction allows to increase the effective number of capacity by 2,0 ÷ 2,5 bits depending on the level of the input signal and the value of the dynamic error, which is achieved by increasing the resolving power of the ADCP. The development of the structure of an analog-digital conversion path with phase-plane correction of dynamic errors, which uses a tabular method for forming signal steepness and a correction member is carried out.

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