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Mathematical model of glitches in DAC with weight redundancy

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ABSTRACT

Glitches appear in digital-to-analog converters and lead to significant limitations of conversion accuracy and speed, which is critical for DAC and limits their usage, especially in the direct digital synthesis systems. This paper researches the causes, the specificity of the appearance of glitches in DAC and the possibility of using weight redundancy in order to reduce glitches in DAC. There had been suggested and analyzed the mathematical model of glitches in DAC with weight redundancy. There had also been proved that glitch amplitude is significantly influenced by the value of the voltage control of the DAC and the parasitic capacities of the digital keys. There had been shown that the attenuation time (duration) of the glitch is significantly influenced by the value of load resistance. The paper shows the expediency of using the DAC based on redundant positional number systems including Fibonacci p-codes. The simulation results prove that with the increase of the parameter p, the characteristics of glitch are significantly improved in comparison with the classical binary system, namely the amplitude and the attenuation time of glitch decrease.

Keywords: DAC, glitches model, weight redundancy

1. INTRODUCTION

Digital to Analog Converters (DAC) are integral components of direct digital synthesis (DDS) devices[1]. DAC determines the accuracy of the output analog signal. It should also be noted that the vast majority of scientific papers on this subject describes the principles of analog signal synthesis and implementation of digital part of the systems. However, the analysis of static and dynamic characteristics of DAC is not reflected sufficiently. This will certainly lead to the simplified perception of DDS devices capabilities and unjustified overstatement of the achievable output parameters. Another negative factor here is glitches.

Glitches are transient pulse tails of output signal A_{out} that occur during changing the DAC input code. The impact of these pulse tails on the waveform significantly increases with the increase in the frequency of the code change $k_{in.}$ For choice of approaches that are used for reduce glitches, it is extremely important to understand the causes and factors that lead to the appearance of glitches in DAC.

There are some modern original researches dedicated to the analysis and modeling of glitches in the DAC[2,3], but they suffer a drawback that all simulations are performed for the case of the switching only one (single) bit. This limitation does not allow to evaluate the behavior of glitches with the increase in switching bits number. However, exactly in these cases, the effect of glitches is appreciably increasing which in turn affects the accuracy, speed and other characteristics of the DAC and especially the devices and systems where they are used. Another disadvantage of existing research [4,5] is that they analyze only one cause of the appearance of glitches, ignoring others, which leads to significant limitations in the use of results[6,7].

2. RESEARCH OBJECTIVES

The objective of researches that are described in this article is to make and analyze the mathematical model of glitches in DAC with weight redundancy, and also to have the possibility of its application for reduce the level of glitches.

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The indicated mathematical model must allow to evaluate the time of action and the amplitude of the output signal during switching of bits DAC depending on various factors such as parameters of key elements, number of bits, amplitude of control signals and load resistance.
As output results next objectives can be considered:

- To consider the causes and the specificity of the appearance of glitches in DAC with weight redundancy.
- To analyze the suggested mathematical model in order to apply it for reducing glitches in DAC with weight redundancy.
- To provide recommendations regarding reducing glitches in DAC with weight redundancy.

3. THE ANALYSIS OF GLITCH ERROR

The appearance of glitches has a very negative impact on both performance and the conversion accuracy and can lead to the significant errors and distortion of the output DAC signal. Generally speaking, glitches can have a pretty complex form, but the most important parameters are the amplitude and the attenuation (stabilization) time of the glitch[8]. As long as glitches appear at the DAC bits switching moment (code combinations changing), the amplitude of the glitch depends on the simultaneous influence of a number of factors, including:

- the total number of bits in DAC,
- the number of bits that are switched for 1 conversion cycle,
- on/off asynchrony of digital keys,
- "parasitic" characteristics of elements of digital keys, in particular capacities in open-circuited mode,
- characteristics of the number system on the base of which the DAC is made,
- conversion algorithm,
- specific value of the control signal (voltage or current),
- DAC load resistance.

The generalized structural scheme of the system of simple direct digital synthesizer of analog signal (A_{out}) based on DAC with weight redundancy (α-DAC) is shown in Fig.1.

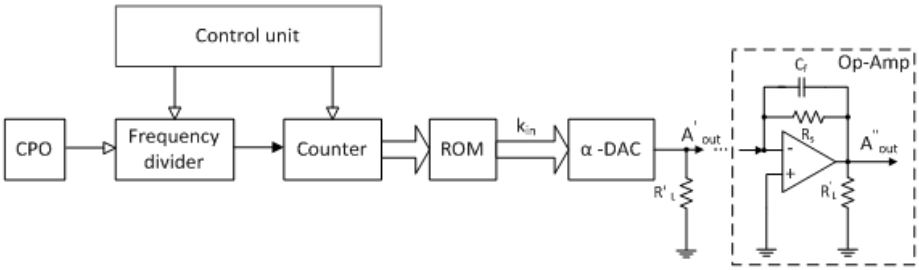

Figure 1. Generalized structural scheme of the system of simple digital synthesizer based on DAC with weight redundancy.

It contains clock-pulse oscillator (CPO), Control unit, Frequency divider, Counter, DAC based on the number system with weight redundancy (α-DAC)[9,10]. In this scheme frequency divider is intended to modify the rate of change of the input signal $\nu = \frac{A_{\max}}{T}$, where T is the time period during which the output signal reaches the set amplitude. The ROM stores the codes of the corresponding generated values (for example, a sinusoid or a signal that monotonically increases/decreases) and the counter forms the corresponding address code for the ROM. The value of signal k_{in} comes from the ROM on the α-DAC. In general, the α-DAC output (with the load resistor R'_L connected) directly can be an output A'_{out} of the DDS system. However, in order to increase the output capability it is expedient to connect to the α-DAC output an operational amplifier (Op-Amp), that has a low input resistance, where C_F is a filter capacitor, R_S is a scale resistor, and R''_L is a load resistor. This allows further improving the characteristics of the DDS system.

4. MATHEMATICAL MODEL OF GLITCHES IN DAC WITH WEIGHT REDUNDANCY

It should be noted that the appearance of glitches in DAC leads to the significant distortions of the output signals A_{out}, which in turn notably limits the possibilities of using the DDS system.

Fig. 2 shows the glitch that appears during 1-bit DAC switching, where the actual signal is represented with the solid line whereas the ideal one is the dotted line.

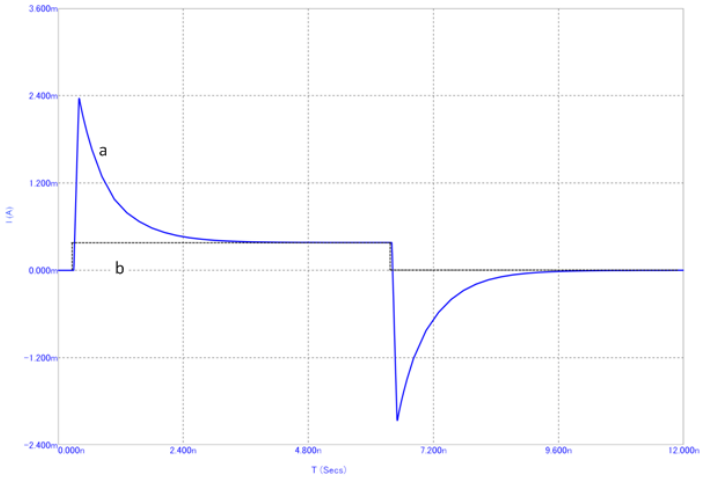

Figure 2. Glitches that appears in the DAC during the switching of the bit: (a) the actual signal; (b) the ideal signal.

The glitch model can be divided into two parts. The first one is a peak of the output signal, which appears from the asynchronous switching of the discharges[11]. Authors consider the use of weight redundancy to be an effective approach to reduce glitches in DAC. This method is independent of specific hardware and the environment parameters and does not require a significant amount of additional equipment.

The worst case occurs when the highest bit has been already turned on, but the lower bits haven't been turned off yet, meaning the DAC output signal equals the sum of the bits, and the glitch value A_{gl} is defined as the sum of bits that are being turned off.

In case of classical binary number system for n-bit DAC the maximum number of bits that can be switched simultaneously equals *n*-1, that is the maximum pulse occurs while changing the code combination from 011...11 to 100...00, that is

$$A_{gl} = Q_{n-1} - Q_0 . \tag{1}$$

In case of changing the code combination from 100…00 to 011…11, that is:

$$A_{gl} = Q_{n-1} , \tag{2}$$

where Q_0 is the value of the *i*-th bit.

It is necessary to note that for the analysis of DAC characteristics the relative glitch value δA_{gl} is more important than the absolute one, and can be calculated as ratio of absolute value to the conversion range

$$\delta A_{gl} = \frac{A_{gl}}{D(n)} . \tag{3}$$

For the classical binary number system the maximum glitch value is equal:

$$\delta A_{gl} = \frac{Q_{n-1}}{D_2(n)} = \frac{2^{n-1}}{2^n} = \frac{1}{2}, \tag{4}$$

otherwise, 50% of the range conversion.

The use of redundant positional number systems (RPNS) allows to significantly reduce the number of bits that are switched simultaneously (especially in multibit DAC) comparing to the binary number system, and thus to reduce the amplitude of the glitch.

An example of RPNS with the whole number weights can serve the number systems based on Fibonacci p-numbers when

$$N = \sum_{0}^{n-1} a_i \varphi_i(i), \tag{5}$$

where $\varphi_p(i)$ – weight of the i-th bit, which equals the i-th Fibonacci p-number[8]. When $p \geq 0$, Fibonacci p-numbers can be calculated by the following recurrence relation:

$$\begin{cases} 0, & \text{when} \quad i < 0 \\ \varphi_p(i) = 1, & \text{when} \quad i = 0 \\ \varphi_p(i-1) + \varphi_p(i-p-1), & \text{when} \quad i > 0 \end{cases}. \tag{6}$$

When $p = 0$, $\varphi_p(i) = 2\varphi_p(i-1)$ and the above representation for N shall be degenerated into a binary system. When $p = 1$, there appears a classical Fibonacci number system.

Table 1 presents the coding of 6-bit DAC based on classical Fibonacci *p*-numbers for $p = 1$ for cases when the maximum possible number of bits are being switched. Conversion range uses 6 bits and its conversion range equals 33 less-significant bit (LSB) equivalent that corresponds to 5 binary bits. Here, the relative value of glitch is:

$$\delta A_{gl} = \frac{A_{gl}}{D(n)} = \frac{Q_{n-1}}{D(n)} = \frac{13}{33} \approx 39\%. \tag{7}$$

Table 1. The value of glitches for 6-bit Fibonacci code for p = 1.

N	**Weight of bit**						A_{gl}	δA_{gl}
	13	8	5	3	2	1		
12	0	1	0	1	0	1	12	37%
13	1	0	0	0	0	0		
13	1	0	0	0	0	0	13	39%
12	0	1	0	1	0	1		

Table 2 presents the coding of 8-bit DAC based on classical Fibonacci p-numbers for p = 2. In this case the relative value of glitch is:

$$\delta A_{gl} = \frac{A_{gl}}{D(n)} = \frac{Q_{n-1}}{D(n)} = \frac{19}{58} \approx 33\%. \quad (7)$$

Table 2. The value of glitches for 8-bit Fibonacci code for p = 2.

N	Weight of bit								A_{gl}	δA_{gl}
	19	13	9	6	4	3	2	1		
18	0	1	0	0	1	0	0	1	18	31%
19	1	0	0	0	0	0	0	0		
19	1	0	0	0	0	0	0	0	19	33%
18	0	1	0	0	1	0	0	1		

There are some other published papers [12,13], dedicated to a detailed analysis of this part of the glitch that appears due to the asynchronous switching of the bits and the method of reduction its influence, where the possibility and efficiency of the use of DAC based on systems with the weight redundancy had been proved and evaluated.

The second part of the glitch appears due to the imperfection of the elemental base of the DAC, in particular the presence of parasitic capacities, as well as the non-ideality of switching elements, resulting in the control signals permeate into the load. Consider this component in more detail.

In order to research the glitch appearance mechanism, a current-steering DAC based on diode switches has been selected. A simple 1-bit current-steering DAC, where switches are implemented based on diode-connected transistors is shown in Fig. 3a.

The equivalent circuits for the switched-off and switched-on states are shown on Fig. 3b and Fig. 3c respectively.

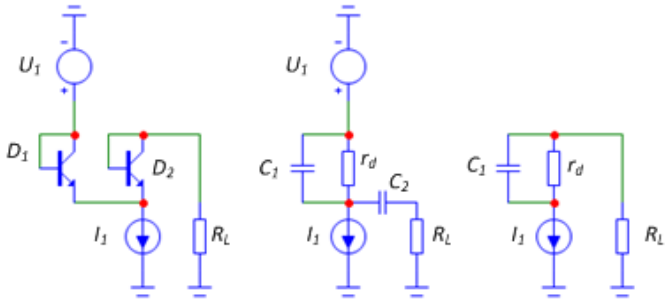

Figure 3. 1-bit current-steering DAC based on diode switches: (a) circuit diagram; equivalent circuits for the switched-off (b) and the switched-on (c) states.

It should be noted that the modelling of glitches for a 1-bit DAC has certain disadvantages since it does not take into account the mutual influence of bits that are being switched simultaneously. Therefore, the study of the glitches appearance mechanism is proposed to perform for a 3-digit DAC.

Fig. 4 represents the circuit of 3-digit current-steering DAC based on diode switches, which are implemented based on diode-connected bipolar transistors.

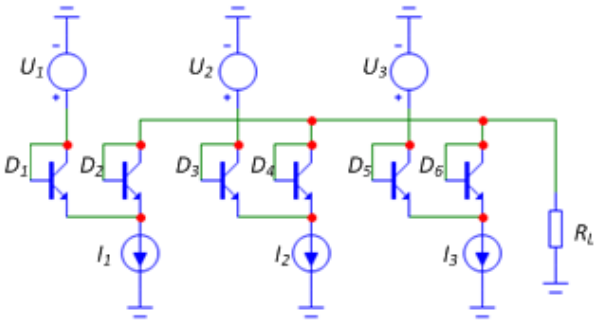

Figure 4. 3-digit current-steering DAC based on diode switches.

Since the highest amplitude of glitch appears in case when all bits of binary or α-DAC are being switched simultaneously, moreover the worst case occurs when the highest bit changes its value, so it is reasonably to perform the modeling exactly for this case. The glitch and the time diagrams of 3-digit current-steering DAC (Fig. 4) in the switching moment of voltage on the control sources V1, V2, V3 are shown in Fig.5.

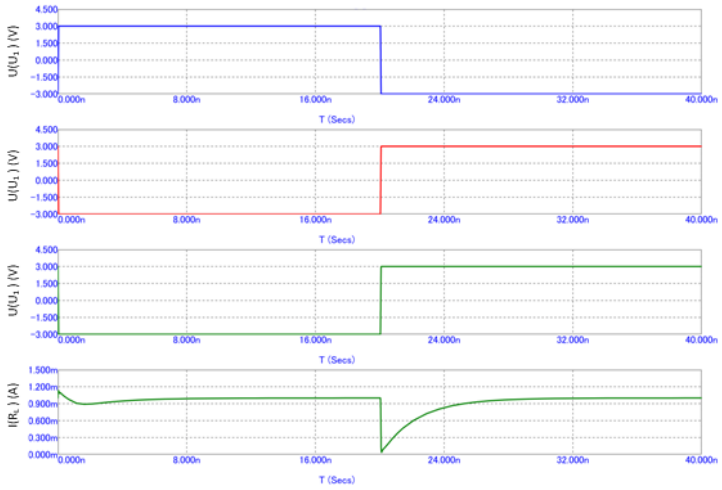

Figure 5. 3 The appearance of glitch in 3-bit current-steering DAC in the switching moment.

Figure 6 shows a fragment of a state of a 3-digit DAC at the time when the highest bit is being turned off, and two low ones are being switched on. Since the identical integrated transistors in the initial DAC circuit are used, the equivalent circuits of these transistors have identical parameters. Therefore, in order to simplify the calculations, it can be assumed that C1 = C2 = C3 = C4 = C.

For the diagram shown in Fig. 6, using the first Kirchhoff's law in operator form, the following equations can be made:

For node A:

$$i_1(s)+i_2(s)=\frac{I_1}{s}+\frac{I_2}{s}+\frac{I_3}{s}\,.. \tag{7}$$

where $i_1(s)$ is the operator current on the segment of AD, $i_L(s)$ – is the operator current on the resistor R_L and a $\frac{I_1}{s}$, $\frac{I_2}{s}$, $\frac{I_3}{s}$, operator currents at the sources current I_1, I_2 and I_3 respectively.
For node B:

$$i_L(s)+i_2(s)=\frac{I_2}{s}+\frac{I_3}{s}. \tag{8}$$

It should be noted that here under the operator resistance, voltage or current, the corresponding values transformed into Laplace domain is meant.

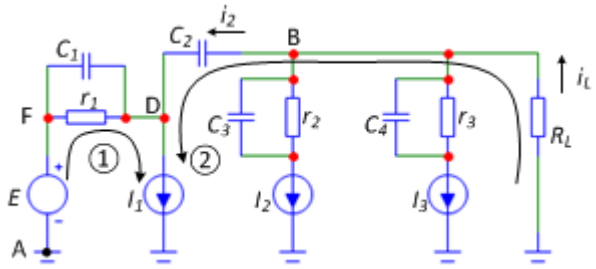

Figure 6. 3-bit current-steering DAC based on diode switches. The equivalent circuit in the highest-bit switching moment.

Since the operator resistance of the condenser is equal to $\frac{1}{sC}$, then the operator resistance of the section of the FD is defined as:

$$z_1(s)=\frac{r_1\frac{1}{sC}}{r_1+\frac{1}{sC}}. \tag{9}$$

For the circuit shown in Fig. 7, using the second Kirchhoff's law in operator form, the following equations can built up:
For the first circuit (1):

$$i_1(s)z_1(s)+U_{I_1}(s)=\frac{E}{s}, \tag{10}$$

where $U_{I_1}(s)$ - is the operator voltage at the current source I1, and $\frac{E}{s}$ - is the operator voltage at the voltage source E.
For circuit (2):

$$i_L(s)R_L+i_2(s)\frac{1}{sC}+U_{I_1}(s)=0. \tag{11}$$

Consequently, we have the following system of equations in operator form:

$$\begin{cases} i_1(s)+i_2(s)=\dfrac{I_1}{s}+\dfrac{I_2}{s}+\dfrac{I_3}{s} \\ i_L(s)+i_2(s)=\dfrac{I_2}{s}+\dfrac{I_3}{s} \\ i_1(s)+z_1(s)+U_{l_1}(s)=\dfrac{E}{s} \\ i_L(s)R_L+i_2(s)\dfrac{1}{sC}+U_{l_1}(s)=0 \end{cases}. \tag{12}$$

The expression (7) leads to:

$$i_1(s)=\frac{I_1}{s}+\frac{I_2}{s}+\frac{I_3}{s}-i_L(s). \tag{13}$$

Analogically from the expression (8) we get:

$$i_2(s)=i_L(s)-\frac{I_2}{s}-\frac{I_3}{s}. \tag{14}$$

From the expression (10) we have:

$$U_{l_1}(s)=\frac{E}{s}-i_1(s)z_1(s). \tag{15}$$

Substituting the value of expression (11) and performing necessary transformations, we can convey the output current in the load resistance as follows:

$$i_1(s)=\frac{\left(\dfrac{I_1}{s}+\dfrac{I_2}{s}+\dfrac{I_3}{s}\right)z_1(s)+\left(\dfrac{I_2}{s}+\dfrac{I_3}{s}\right)\dfrac{1}{sC}-\dfrac{E}{s}}{R_L+\dfrac{1}{sC}+z_1(s)}. \tag{16}$$

Since the values of r_1 and C in equations (9) and (16) are constant and depend on the selected element base, and the values I_1, I_2 and I_3 specify the values of the corresponding DAC digits, then only the changes of value load resistance R_L and the voltage of control source E can essentially have an influence to the change of output signal of DAC. It should be noted that the range of change in control voltage E is also significantly limited, so only a change in the value of the load resistance of the circuit might have a significant effect on the glitch.

In order to analyze the formula (16), namely for the inverse Laplace transformation, the software package MathCAD 15 was used. The graphic representation of the simulation result for the values E =1V and R_L =100Ω is shown on figure 7.

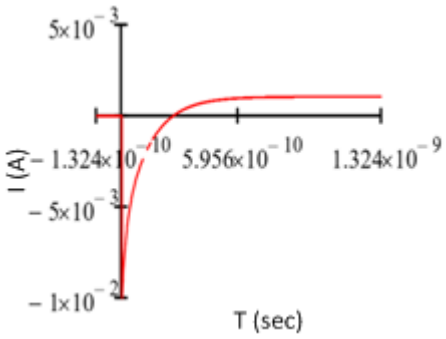

Figure 7. The result of simulation of glitch in 3-digit current-steering DAC.

Table 3 shows the value of the glitch amplitude and its duration for some values of the output resistance R_L .

Table 3. Values of amplitude and duration of a glitch in a 3-digit DAC for some values of the output resistance

R_L, Ω	10	20	50	100	150	200	300	500	750	1000
t_{set}, ns	0,22	0,25	0,44	0,77	1,08	1,35	1,85	2,95	4,3	6,3
I, mA	-100	-50	-20	-10	-7	-5	-3,3	-2	-1,25	-1

Obtained results show that with the increase of load resistance value R_L the glitch amplitude decreases but the time of the output signal setting, meaning the attenuation duration of the glitch, significantly increases, that critically affects on DAC performance. The graphs attenuation duration of the glitch, and the glitch amplitude in the DAC versus the load resistance are shown in Fig. 8a and Fig. 8b respectively.

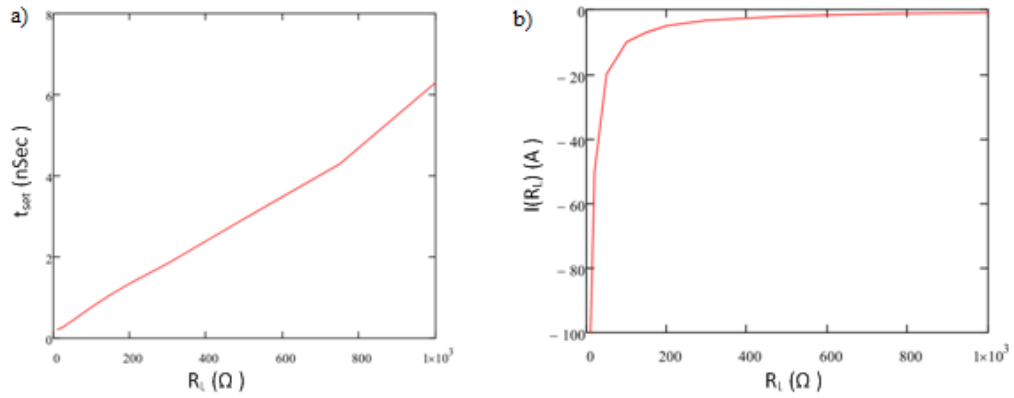

Figure 8. Glitch parameters vs. load resistance graphs in current-steering DAC: a) the duration of the glitch; b) the amplitude of the glitch.

The graphs shows that the duration of the glitch depends on the load resistance almost linearly, whereas the dependence of the glitch amplitude from R_L has a logarithmic character.

5. SIMULATION RESULTS

The adequacy of the proposed mathematical model is confirmed by the computer simulation, which was performed in the integrated package Micro-CAP 10 using the models of integrated transistors NUHFARRY.

Figure 9a shows the glitches in the DAC at the moment when the highest bit is being turned off, depending on certain values of the load resistance values R_L from the Table 3. The simulation proves that with the increase of the resistance R_L , the attenuation time of the glitch also increases.

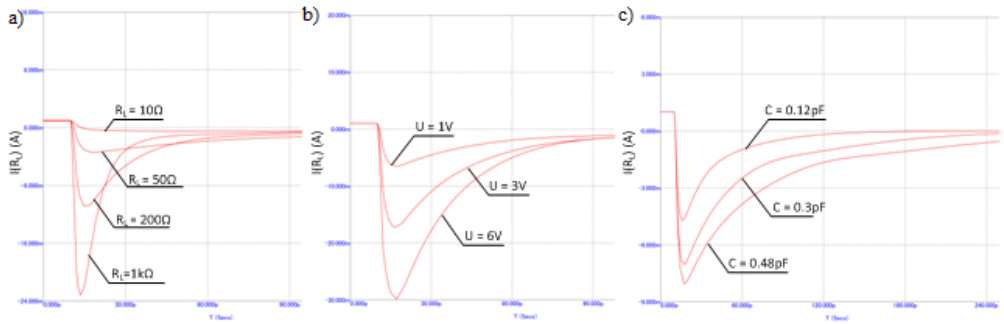

Figure 9. Glitches in current-steering DAC depending on (a) resistance R_L, (b) the voltage source of control, (c) the parasitical capacity of diode switches.

Glitches depending on different values of the source control voltage of the DAC at the highest bit switching moment are shown in Fig. 9b. The simulation proves that the increase of the source control voltage leads to the both glitch's amplitude and attenuation time increase.

Fig. 9c presents the glitches at the moment when the highest bit is being turned off for different values of the parasitical base-to-emitter capacity of the selected transistors models which are used as diode switches of DAC. The simulation was performed within the range of -50% to +100% of the specified value of the NUHFARRY bipolar transistor model from the component's library of the software package Micro-CAP 10. The obtained results prove that increase of the value of parasitic capacities leads to the increase of both amplitude and the attenuation time of glitches.

The important factor that affects glitches characteristics is also the number of bits, which are being switched simultaneously, moreover, the bigger the level of them, the bigger the amplitude of the glitch. In case of classical binary number system, the worst case appears when all digits are being switched simultaneously. The use of redundant positional number system in particular RPNS based on the value of golden p-ratio and Fibonacci numbers [8,9], allows to limit the number of bits that are being switched simultaneously, which in turn leads to a significant decrease in the amplitude of the total glitch.

Figure 10 shows the result of the simulation of glitches in the DAC, implemented based on the p-numbers of Fibonacci, which confirms the fact that the use of RPNS leads to a significant reduction of glitches in the DAC.

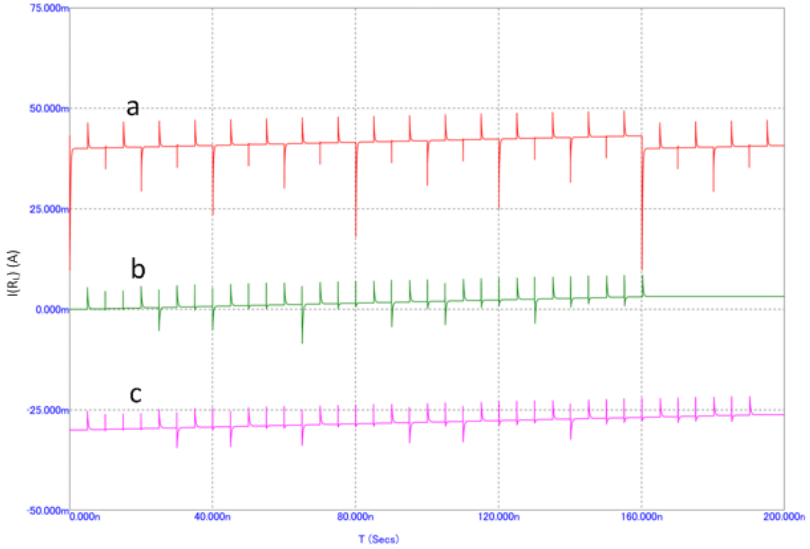

Figure 10. The glitches in n-digit DAC on basis of (a) classical binary system number; (b) Fibonacci code for p = 1; (c) Fibonacci code for p = 2.

There is another published paper[10] dedicated to the investigation of the glitches depending on the "analog-to-digital" converting algorithm and the possibility of RPNS use in order to decrease them. That paper analyses the properties of various redundant positional numerical systems in detail. The structural diagram of the DAC based on the number system with weight redundancy was also proposed by the authors[11,12,13].

It should be noted that the load resistance at the output of the DAC R_L is determined by the practical use of DAC. Thus, in the DDS system is shown in Fig. 1 it is advisable to connect a push-pull symmetric current amplifier [14] to the output of the DAC, for example, proposed by the authors[15]. It has a low input resistance, which significantly reduces the attenuation time of the glitch. The use of the amplifier also allows to reduce the voltage in the control circle of the DAC, which in turn leads to additional reduction of the glitch amplitude.

6. CONCLUSIONS

Attempting glitches in digital-to-analog converters lead to significant limitations of conversion accuracy and speed, parameters. This paper focuses both on causes, as well as the specificity of the appearance of glitches in DAC. Some methods of their reduction are proposed.

The paper presents the causes and the specificity of the appearance of glitches in α-DAC with weight redundancy. There had been shown that the appearance of glitches in DAC considerably limits the possibilities of its use, especially in the direct digital synthesis systems.

The mathematical model of glitches in α-DAC was suggested and analyzed. There had been proved that glitch amplitude is significantly influenced by the value of the voltage control of the DAC and the parasitic capacities of the digital keys. Additionally, authors shown that the attenuation time (duration) of the glitch is significantly influenced by the value of load resistance.

The expediency of using the DAC based on RPNS had been shown. There had been proved that with the increase of the parameter p, the characteristics of glitch are significantly improved, namely the amplitude and the attenuation time of glitch decrease.

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