Consumer and Corporate Affairs Canada | Consommation et Corporations Canada

(11) (A) No. 1 165 889

(45) ISSUED 840417

(52) CLASS 354-98

(51) INT. CL.[3] H03K 13/02

(19) (CA) **CANADIAN PATENT** (12)

(54) CONVERTER FOR CONVERTING P-CODES INTO ANALOG VALUES

(72) Stakhov, Alexei P.;
Azarov, Alexei D.;
Moiseev, Vyacheslav I.;
Uzhvak, Jury N.;
Vekhovoi, Viktor P.,
USSR

(73) Granted to Vinnitaky Politekhnichesky Institut
USSR

(21) APPLICATION No. 358,107

(22) FILED 800812

No. OF CLAIMS 1

Canada

DISTRIBUTED BY THE PATENT OFFICE, OTTAWA.
CCA-274 (11-82)

CONVERTER FOR CONVERTING P-CODES INTO ANALOG VALUES

ABSTRACT OF THE DISCLOSURE

The proposed converter comprises means for code permutation, means for separating a difference between output signal levels, means for storing numbers of faulty positions, means for selecting a type of permutation, and control means, which means when taken in a combination provide for determining numbers of faulty positions accurate to one bit position, and for correct conversion of a digital value into an analog equivalent in a case of the presence of a certain number of faulty positions in the converter, said conversion being based upon the main relationships between the code bit position weights of a final golden proportion, and Fibonacci p-codes.

The present invention relates to the art of computations and measurements, and particularly to a converter for converting p-codes into analog values.

Herein the term "p-codes" designates Fibonacci p-codes and codes of a golden proportion.

The present invention may prove most advantageous in digital measuring instruments, for example when measuring electrical values. Moreover, it is utilized in automatics and telecontrol to convert outputs produced by a control means into the control instructions transferred to actuating means, and also in radio-lecation and in electron-ray instruments to control scanning of the electron ray.

Any analog-to-digital converter must be subjected to metrological checking so as to be sure that its metrological characteristics correspond to the required values. To accomplish such checking, a large set of samples is required, which is rather difficult to practice. Moreover, the process of metrological checking itself requires significant time expenses.

Known in the art is a converter for converting p-codes into analog values (see A. P. Stakhov, Vvedenie Vvedenie v algoritmericheskuyu teoriyu izmereniya, Moscow, Sovetskoye radio, 1977, p. 177), comprising key elements corresponding in number to that of code positions. Each of the key elements is connected with its output to a corresponding input of

an adder of sample analog values being proportional to the weights of code positions. Inputs of the key elements are the input of the prior art converter, while the output thereof is the output of the adder for sample analog values.

The prior art converter operates as follows.

Signals corresponding to the bit positions of the code being converted, are fed to the inputs of the key elements. In their turn, those key elements at whose inputs there arrive signals corresponding to ones in the code being converted, connect corresponding sample values whose sum represents an output analog value.

Metrological checking of such a converter is a rather complicated operation. To accomplish this checking, a large number of sample values difficult to practice, is required. Moreover, the prior art converter possesses a low reliability because in the case of a metrological fault of at least one bit this converter does not meet the required metrological characteristics (conversion accuracy, linearity of the output characteristic etc.).

The main object of the present invention is the provision of a converter for converting p-codes into analog values, wherein the utilization of the ambiguity of code representation of the same number ensures carrying out metrological checking and increasing the performance reliability thereof.

Another object of the present invention is to increase the percentage of the yield of efficient products in mass production of the given converter in the form of a large-scale integration circuit.

In accordance with a particular embodiment of the invention there is provided a converter for converting p-codes into analog values. The converter includes means for code permutation, intended for storage and permutation of input codes in a point-to-point conversion mode, and also codes corresponding to the weights of bit positions being checked in a metrological check mode. Key elements corresponding in number to that of the code positions are controlled by output signals of the above means for code permutation. Means for adding sample analog values are proportional to the weights of code positions and actuated by the key elements, an output of the means for adding being an output of the converter. Means for providing a difference between output signal levels of the means for adding sample analog values, have an output signal indicative of the presence of faulty positions. Means for storing numbers of faulty positions determined by a signal indicative of the presence of faulty positions which signal is fed from an output of the means for providing the difference are also provided as are the means for selecting a type of permutation and allowing to determine the type of permutation effected by the means for code permutation on a signal fed from the means for storing.

Inputs of a control circuit are applied to switch signals for selecting converter operation modes and signals indicative of the presence of faulty positions in a point-to-point input conversion mode and also in a metrological check mode, while outputs of the control circuit provide for required interaction between the means for code permutation, the means for providing a difference and the means for storing in a predetermined operation mode.

Such an embodiment of the inventive converter allows metrological checking thereof to be simplified, and performance reliability to be increased.

The objects set forth and other objects and advantages of the present invention are further explained by a detailed description of an illustrative embodiment of the present invention with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of the converter for converting p-codes into analog values of the invention;

Fig. 2 is a modification of the unit for determining a type of the permutation.

The converter for converting p-codes into analog values comprises key elements 1 corresponding in number to that of code positions. Each of the elements 1 is connected with its output to a corresponding input of an adder 2 for summing

sample values proportional to the weights of code positions.

The adder 2 may be, for example, constructed as a source of weighted currents.

An output 3 of the adder 2 is the output of the converter being described, while a multiposition output 4 of this adder 2 is connected to a first multiposition input of the elements 1.

According to the invention, the converter is provided with a unit 5 for code permutation, a unit 6 for extracting a difference between output signal levels of the adder 2, a unit 7 for storing numbers of faulty stages, a unit 8 for determining a type of the permutation, and a control unit 9.

The unit 5 for code permutation is intended for storing and permutation of the input codes in a point-to-point conversion mode, and also for storing and permutation in codes corresponding to the weights of the positions being checked in a metrological check mode.

The unit 5 in the preferred embodiment is a device for reducing Fibonacci p-codes to a minimum form (British Patent Specification No. 1,543,302).

A first multiposition input 10 of the unit 5 is the multiposition input of the proposed converter.

A second multiposition input 11 of the unit 5 is connected to a second multiposition output of the unit 7.

The unit 7 in the modification being described is a register providing for storing numbers of faulty stages.

It should be noted that a stage fault may be of two kinds.

First, when a sample value cannot be completely utilized for forming an output analog value, there exists a "out of service" type fault (a disastrous fault).

Secondly, when a sample value which forms an output analog signal, is not proportional to the weight of the code position, there exists an "up-setting" type fault (a parameter fault).

The first multiposition output of the unit 7 is connected to a multiposition input 12 of the unit 9 and to a first multiposition input 13 of the unit 8, which unit is connected with its second multiposition input 14 to a multiposition output of the unit 5, the multiposition output of the unit 5 being also connected to a second multiposition input 15 of the elements 1.

The unit 8 has its output connected to a first input 16 of the unit 9.

The unit 9 further has a control input 17 to which input switch signals of operation modes of the converter are fed from an external control unit (not shown in the drawing).

The unit 9 has its first output connected to a control input of the unit 5, while a second output thereof is connected to a control input 19 of the unit 7, and a third output thereof is connected to a control input 20 of the unit 6, which unit is connected with its input to the output 3, while an output thereof is connected to an input 21 of the unit 7, and to a second input 22 of the unit 9.

Thus, the control unit 9 whose inputs are fed with switch signals of operation modes of the converter, and with signals indicative of faulty positions in a point-to-point conversion mode, and also in a metrological check mode, makes it possible to execute the necessary interaction between the units 5, 6 and 7, in a predetermined operation mode.

The units 6 whose output signals is indicative of the presence of faulty position, may be a differencing unit, while the unit 8 allowing to determine the type of permutation effected by the unit 5 from a signal being fed from the unit 7, may be a combinational logic circuit of the type shown in Fig. 2.

In this case the unit 8 comprises logic AND circuits 23 corresponding to number "n" of the code positions, an output of each circuit 23 being connected to a corresponding input of an OR circuit 24, an output of the latter being the output of the unit 8. First inputs of the circuits 23 form the first multiposition input 13 of the unit 8, while second inputs thereof form the second multiposition input 14 of said unit 8.

The inventive converter has two operation modes a metrological check mode and a point-to-point conversion mode for converting a p-code into an analog value, while the first mode must precede the second one, and switching operation modes is effected by an instruction fed to the control input 16.

As it has been above indicated, p-codes includes Fibonacci p-codes and codes of the golden p-proportion.

Fibonacci p-code is a representation of any natural number N in the following form:

$$N = \sum_{i=0}^{n} a_i \varphi_p(i), \qquad (1)$$

where $a_i \in \{0,1\}$;

U_p is the weight of the ith bit or the ith Fibonacci p-number which is calculated as follows:

$$U_p(i) = \begin{cases} 0, & \text{if } i < 0 \\ 1, & \text{if } i = 0 \\ U_p(i-1) + U_p(i-p-1), & \text{if } i > 0 \end{cases} \qquad (2)$$

The code of the golden p-proportion is a representation of any real number D in the following form:

$$D = \sum_{i=-D}^{+D} a_i \alpha_p^i , \qquad (3)$$

where $a_i \in \{0,1\}$

α_p^i is the weight of the ith bit;

$\alpha_p^i = \alpha_p^{i-1} + \alpha_p^{i-p-1}$.

The following relationship is satisfied for α_p^i

$$\alpha_p^i = \alpha_p^{i-1} + \alpha_p^{i-p-1} . \qquad (4)$$

There exists a plurality of representations of the same number in the form shown in (1) and (3), among said representations being also such wherein not least than p

zeroes are present to the right of each one. Such a form of representation is called minimal. The transfer from the minimal form to any other form of representation of a p-code is achieved through code permutation, which operation is based upon the relationships (2) and (4). The code permutation consists in the substitution of a one of the ith position for ones in the (i-1)th and (i-p-1)th positions, which substitution is effected in the case of the presence of zeroes in the latter. The feature of the above operation consists in that it does not change the value of the number being represented by the code, while changing only the code pattern. The code permutation is designated $\Lambda\!\!\uparrow$.

Metrological checking of the converter for converting p-codes into analog values is based upon checking the main relationships between the bit position weight of said converter, which bit positions when, for example, p=1, are the following:

$$x_1 = x_{1-1} + x_{1-2} \tag{5}$$

$$x_1 = \sum_{i=0}^{\ell-2} x + x'_0 \tag{6}$$

where x'_0 is an additional bit position whose weight is equal to that of a least significant bit position.

$$x_1 = x_{1-1} + x_{1-3} + x_{1-4} \tag{7}$$

Basing upon the relationships (5, 6, 7), the bit positions in the inventive converter are subjected to the permutation of the types I, II, and III, which operations

consists in substituting the one of the ℓ-position for the ones present in the right portions of the equations (5), (6), and (7).

Metrological checking when, for example, p=1, is done as follows.

On command from the control unit 9, a one is placed in the most significant position of the unit 5. Next, from a signal being fed from the block 9, this one is subjected to the permutation of the first type.

In the case of the presence of a faulty state, the relationship (5) is not fulfilled for these stages, and the unit 6 generates a signal which is fed to the units 7 and 9. In the unit 7, ones are recorded each time into two most significant positions taking part in the permutation during which the unit 6 for extracting a difference between output signal levels of the converter operates.

Following each operation cuased by a signal fed from the unit 9, the unit 6 is reset to the initial state. If the unit 6 has not operated a single time during permutation, the control unit 9 produces a signal for the determination of metrological checking, from the signals being fed to the input 12. After the permutation of the first type is over, the unit 9 pro-duces a signal causing the recording of a one into the k-th least significant of expected faulty position, from the block 7 into the block 5. On command from the unit 9, the said one is subjected to the permutation of the firsttype. If the unit 6 operates at this time, the unit 7 records the number

of this position as a faulty one in the form of a one in the k-th position. A one is recorded in the unit 5 into a (k+1)th position, while the unit 8 forms a signal permitting the permutation of the second type. If the unit 6 has not operated during permutation of the k-th one, then the recording of the number of this position does not occur in the unit 7. Next, on command from the unit 9 there take place substitution of the one recorded in the (k+1)th bit position of the unit 5. The type of substitution is determined by the unit 8. If the unit 6 operates during substitution of the one recorded in the (k+1)th bit position of the unit 5, the number of this position is fixed by the unit 7 as a number of a faulty position.

Selection of the type of permutation effected in the unit 8 for determining a type pf permutation during the whole process of metrological checking, is determined depending on the state of the unit 7.

The process of metrological checking of the remaining expected faulty positions is effected in a similar way.

The process of checking the converter of the invention is accomplished to an accuracy of one position if not less than (k+1) most significant correct positions precede each group consisting of m ($1 \leq m \leq p$) successive faulty positions. If the most significant position taken from the group of the faulty position is the most significant position of the converter of the invention, such a condition is unnecessary. In

other cases checking is done to an accuracy of two or three positions with the exception of the (p+1)th least significant of the faulty positions whose numbers are always determined accurate to one position.

An example of metrological checking of the inventive seven-position converter wherein position weights are proportional to p=1 Fibonacci numbers, with the first and the fourth positions being fault, is given in Table 1.

Table 1

Time	Unit 7 state: Position numbers 1 2 3 4 5 6 7 / Position weights 13 8 5 3 2 1 1 1	Unit 6 sample	Type of permutation	Unit 7 state: Position numbers 1 2 3 4 567	Permutation termination signal	Checking termination signal
1	0 0 0 0 0 0 0 0	0		0 0 0 0 000	0	0
2	1 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0	1		1 1 0 0 000	0	0
3	0 1 1 0 0 0 0 0 0 1 0 1 1 0 0 0	1	I	1 1 1 1 000	0	0
4	0 1 0 1 1 0 0 0 0 1 0 1 0 1 1 0	0	I	1 1 1 1 000	0	0
5	0 1 0 1 0 1 1 0 0 1 0 1 0 1 0 1	0	I	1 1 1 1 000	1	0
6	0 0 0 0 0 0 0 0	0		1 1 1 1 000	0	0
7	0 0 0 1 0 0 0 0 0 0 0 0 1 1 0 00	1	I	1 1 1 1 000	1	0
8	0 0 0 0 0 0 0 0	0		1 1 1 1 000	0	0
9	0 0 1 0 0 0 0 0 0 0 0 0 1 1 1 1	0	II	1 1 0 1 000	1	0
10	0 0 0 0 0 0 0 0	0		1 1 0 1 000	0	0
11	0 1 0 0 0 0 0 0 0 0 1 0 1 1 0 0	0	III	1 0 0 1 000	1	0
12	0 0 0 0 0 0 0 0	0		1 0 0 1 000	0	0
13	1 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0	1	I	1 0 0 1 000	1	0
14	0 0 0 0 0 0 0 0	0		1 0 0 1 000	0	1

Metrological checking of such converter is accomplished accurate to one position.

The inventive converter operates in the point-to-point mode for converting a p-code into an analog value as follows.

The control unit 9 inhibits the operation of the unit 6 and enables the operation of the unit 7, 8, and 5.

If there are no faulty positions in the converter, the unit block 9 inhibits the code permutation in the unit 5, and a source digital code given in a minimum form, is fed to the input 10 where it is converted into the analog equivalent in the known way.

If faulty positions occur in the process of metrological checking, the unit 7 sends a signal to the unit 8 which unit generates a signal permitting substitution of ones of the source code in the positions having numbers which coincide with the numbers of erroneous positions fixed in the unit 7. The inventive converter performs the correct conversion of the digital value into the analog equivalent if not less than m+1 least significant correct position follow each group of m ($1 \leq m \leq p$) successive erroneaus position, or if there is not more than one group of (m=p) erroneous positions.

The following condition must be satisfied in the general case:

$$S_n - S_n^* \geq S_p$$

where S_n is a sum of all the weights of the n-position converter

S_n^* is a sum of all the weights of a maximum code combination

S_p is a sum of weights of all the erroneous positions.

An example of conversion of a source p=1 Fibonacci code into an analog equivaltn effected by the eight-position converter, with the first bit position being erroneous, is given in Table 2.

Table 2

Source code	Analog equivalent of the source code	Unit 6 state position numbers	Permutation termination signal
position numbers			
1 2 3 4 5 6 7 8		1 2 3 4 5 6 7	
position weights			
21 13 8 5 3 2 1 1			
1 0 1 0 1 0 1 0	33	1 0 0 0 0 0 0	0
1 0 1 0 1 0 0 1	33	1 0 0 0 0 0 0	0
1 0 1 0 0 1 1 1	33	1 0 0 0 0 0 0	0
1 0 0 1 1 1 1 1	33	1 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	33	1 0 0 0 0 0 0	1

In such a converter, one erroneous bit position does not affect the correct conversion of the source code into the analog equivalent.

Introduction of new units and links provides for an increase in the resolving power of metrological checking to an accuracy of one bit position, and also for an increase in the reliability in converting the source code in the analog equivalent with not more than q bit positions being faulty ("out of service" type). This is achieved by substituting a source minimum code combination for an equivalent combination, using permutation.

In the equivalent code combination faulty positions have no ones, thus allowing the correct analog value of the source code to be obtained.

The latter consideration makes it possible to increase the yield of products in mass production of analog-to-digital converters being large-scale integration circuits due to the fact that converters having not more than q faulty positions can be considered as efficient products.

While the invention has been described herein in terms of specific Examples, which are to be taken as preferred, numerous variations and modifications may be made in the invention without departing from the spirit and scope thereof as set forth in the appended claims.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:-

1. A converter for converting p-codes into analog values, comprising:

- means for code permutation, intended for storage and permutation of input codes in a point-to-point conversion mode, and also codes corresponding to the weights of bit positions being checked in a metrological check mode;
- key elements corresponding in number to that of code positions and being controlled by output signals of the above means for code permutation;
- means for adding sample analog values being proportional to the weights of code positions and actuated by said key elements, an output of said means for adding being an output of said converter;
- means for providing a difference between output signal levels of said means for adding sample analog values, and having an output signal indicative of the presence of faulty positions;
- means for storing numbers of faulty positions determined by a signal indicative of the presence of faulty positions which signal is fed from an output of said means for providing said difference;
- means for selecting a type of permutation and allowing to determine the type of permutation effected by said means for code permutation on a signal fed from said means for storing;
- a control circuit to whose inputs there are applied switch signals for selecting converter operation modes, and signals indicative of the presence of faulty positions in a point-to-point input conversion

mode, and also in a metrological check mode, while outputs thereof provide for required interaction between said means for code permutation, said means for providing a difference, and said means for storing, in a predetermined operation mode.

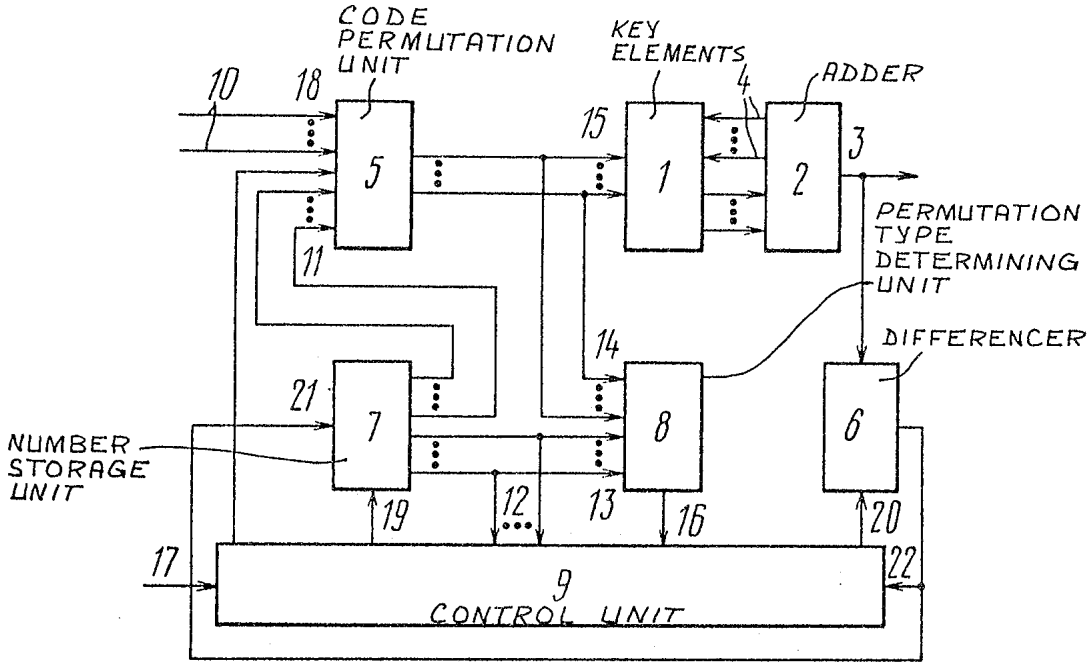
CODE PERMUTATION UNIT
KEY ELEMENTS
ADDER
10
18
15
4
3
5
1
2
11
PERMUTATION TYPE DETERMINING UNIT
14
DIFFERENCER
21
7
8
6
NUMBER STORAGE UNIT
19
12
13
16
20
17
9
CONTROL UNIT
22

FIG. 1

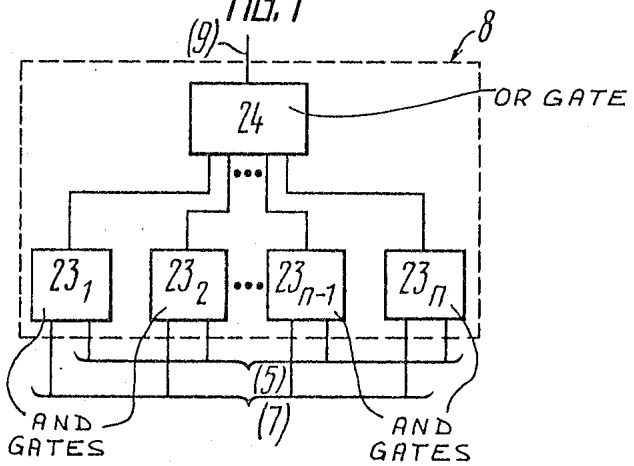
(9)
8
OR GATE
24
23 1
23 2
23 n-1
23 n
(5)
(7)
AND GATES
AND GATES

FIG. 2