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Холявка А.О. 1117
КОМУНІКАТИВНА ВЗАЄМОДІЯ ВИКЛАДАЧА І СТУДЕНТА У ПРОЦЕСІ ПОДОЛАННЯ БАР'ЄРІВ ВИВЧЕННЯ АНГЛІЙСЬКОЇ МОВИ

Шунков В.С., Брюховецька І.В., Задорожна О.М. 1124
ЕЛЕКТРОННІ ПІДРУЧНИКИ ТА ІНТЕРАКТИВНІ ДЖЕРЕЛА ПРИ ВИВЧЕННІ ХІМІЇ

Якименко П.В. 1140
РОЛЬ ВЧИТЕЛЯ У ФОРМУВАННІ ТВОРЧИХ ЗДІБНОСТЕЙ ЗДОБУВАЧІВ ОСВІТИ ПОЧАТКОВОЇ ШКОЛИ

Яременко О.М. 1147
СПОРТИВНО-ОЗДОРОВЧЕ ВІДНОВЛЕННЯ ЯК СКЛАДОВА ДІЯЛЬНОСТІ ВЧИТЕЛЯ ФІЗИЧНОЇ КУЛЬТУРИ В ЗАКЛАДАХ ЗАГАЛЬНОЇ СЕРЕДНЬОЇ ОСВІТИ

СЕРІЯ «Техніка»

Artyukh O.M., Ruban D.P., Tarasenko O.V., Petriuk Yu.I., Ruban H.Ya. 1159
UNMANNED TRANSPORT. MODERN TECHNOLOGIES, CHALLENGES, AND PROSPECTS

Biloivanenko M.V., Biloshytskyi Ya.O. 1199
A DIMENSIONAL APPROACH FOR WEB API TESTING

Furtat I.E., Furtat Yu.O. 1214
INFLUENCE OF THE CHARGED DOUBLE LAYER ON THE KINETICS OF ION ABSORPTION IN A BI-POROUS MEDIUM DURING FABRIC DYEING

Hablovska N. 1222
ANALYTICAL MODEL OF GEOMETRIC PARAMETERS OF PSEUDO-LIQUID METAL CONTACTS AND CONDUCTIVE SURFACE

Kravchuk Ya.Ya. 1232
WEB TECHNOLOGIES FOR DEVELOPING SCALABLE VOLUNTEER PLATFORMS

Kychak V.M., Krasilenko V.G., Nikitovich D.V. 1244
MODELING AND DESIGN OF CODE-CONTROLLED MULTIFUNCTIONAL CONTINUOUS-LOGIC DEVICES, AS A BASIC CELLS OF ADVANCED MIMO-STRUCTURES AND HIGH-PERFORMANCE SENSOR SISTEMS

Nesterenko S.A., Alokhin A.O. 1260
PROCEDURE FOR SELECTING A NETWORK CHANNEL OF THE IEEE 802.3AZ STANDARD FOR HETEROGENEOUS TRANSACTIONS

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MODELING AND DESIGN OF CODE-CONTROLLED MULTIFUNCTIONAL CONTINUOUS-LOGIC DEVICES, AS A BASIC CELLS OF ADVANCED MIMO-STRUCTURES AND HIGH-PERFORMANCE SENSOR SISTEMS

Abstract. The work is devoted to the consideration of the issues of design and modeling of some new hardware implementations of code-controlled smart multifunctional continuous logic devices (SMCLD) with time-pulse representation of operands as improved basic cells of advanced MIMO structures and high-performance parallel-type sensor systems for input, image processing and solving interconnection problems for picture operands. The proposed code-controlled SMCLDs implement, in accordance with the control code, one of the functions of two-valued, multi-valued and continuous logics, in which the input and output operands are represented by currents flowing in current mirrors. As shown in the work, such improved basic cells can additionally implement the functions of nonlinear time-pulse conversion or analog-to-digital conversions and, with some simple modifications, expand the set of other continuous and neural logic functions performed by them, including implementing neuron activation functions. The results of simulations of such elements confirm their following advantages: high speed and reliability, simplicity, low power consumption, high level of integration. The conceptual proposed approach to building SMCLDs consists in using current mirrors implemented on 1.5-μm CMOS transistors. The small number of components required for the implementation of the basic cell, namely from 50 to 70 transistors, 1 photodiode and 1 LED, makes the proposed circuits quite compact. The simulation

results of such basic functions as NOT, MIN, MAX, equivalence (EQ), normalized summation, averaging and others, which were implemented by such SMCLDs, showed that the level of logical variables can vary from 0.1 μA to 10 μA for low-power variants. SMCLDs have low power consumption <1 mW and processing time of about 1÷11 μs at a supply voltage of 2.4÷3.3 V.

Keywords: Smart multifunctional continuous logic devices, parallel high-performance processing, sensor with MIMO-structure, time-pulse coding, equivalence and nonequivalence operations, matrix continuous logic, photocurrent mirror.

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МОДЕЛЮВАННЯ ТА ПРОЕКТУВАННЯ БАГАТОФУНКЦІОНАЛЬНИХ ПРИСТРОЇВ З НЕПЕРЕРВНОЮ ЛОГІКОЮ З КОДОВИМ КЕРУВАННЯМ, ЯК БАЗОВИХ ЕЛЕМЕНТІВ УДОСКОНАЛЕНИХ МІМО-СТРУКТУР ТА ВИСОКОПРОДУКТИВНИХ СЕНСОРНИХ СИСТЕМ

Анотація. Робота присвячена розгляду питань проектування та моделювання деяких нових апаратних реалізацій кодокерованих інтелектуальних багатофункціональних неперервно-логічних пристроїв (ІБНЛП) з часоімпульсним представленням операндів, як удосконалених базових комірок удосконалених МІМО-структур та високопродуктивних сенсорних систем паралельного типу для введення, обробки зображень та вирішення проблем міжз'єднань для картинних операндів. Запропоновані кодокеровані ІБНЛП реалізують у відповідності коду керування одну з набору функцій двозначних, багатозначних та неперервних логік, у яких вхідні та вихідні операнди представлені струмами, що протікають в віддзеркалювачах струму. Як показано в роботі, такі удосконалені базові комірки додатково

можуть реалізувати функції нелінійного часо-імпульсного перетворення чи аналого-цифрових перетворень та при деяких простих модифікаціях розширити набір виконуваних ними інших функцій неперервних та нейронної логік, в тому числі реалізувати функції активації нейронів. Результатами моделювань таких елементів підтверджені такі їх переваги: висока швидкість та надійність, простота, мале енергоспоживання, високий рівень інтеграції. Концептуальний пропонований підхід до побудови ІБНЛП полягає у використанні струмових дзеркал, реалізованих на 1,5-мкм CMOS-транзисторах. Невелика кількість необхідних для реалізації базової комірки компонентів, а саме наявних від 50 до 70 транзисторів, 1 фотодіода та 1 світлодіода робить запропоновані схеми досить компактними. Результати моделювання таких основних функцій, як NOT, MIN, MAX, еквівалентності (EQ), нормалізованого підсумовування, усереднення та інших, що були реалізовані такими ІБНЛП, показали, що рівень логічних змінних може змінюватися від 0,1 мкА до 10 мкА для варіантів з низьким енергоспоживанням. ІБНЛП мають низьке енергоспоживання <1 мВт та час обробки близько 1÷11 мкс при напрузі живлення 2,4÷3,3 В.

Ключові слова: Інтелектуальні багатофункціональні пристрої неперервної логіки, паралельна високопродуктивна обробка, датчик з MIMO-структурою, часо-імпульсне кодування, операції еквівалентності та нееквівалентності, матрична неперервна логіка, фотострумове дзеркало.

Introduction. More than ten years the use of optical interconnects is discussed as an alternative to solve the mentioned problems on interconnect in VLSI technology. A lot of demonstrator systems were built to prove the use of optics or optoelectronics for off-chip and on-chip interconnects [1]. At present the situation for smart detector circuits is much easier. They can be regarded as a subset of OE-VLSI circuits because they consist only of arrays of photo-detectors with corresponding evaluation circuit for analogue to digital converting. The latter's can be realized not only in GaAs technologies, but in Silicon [2]. The strategic direction of solution of various scientific problems becomes fast-acting and parallel processing of large arrays (2-D) of data using non-conventional computational MIMO-systems, corresponding matrix logics and corresponding mathematical apparatus [3-8]. For numerous perspective realizations of optical learning neural networks (NN) with two dimensional structure [3], of recurrent optical NN [4], of the continuous logic equivalency models (CLEM) NN [5-7], the elements of matrix logic are required, and not only of two-valued, but also continuous, neural-fuzzy logics. Advanced parallel computing structures and MIMO-systems require both parallel processing and parallel information input/output. Generalization of scalar two-valued logic on matrix case has led to intensive development of binary images

algebra (BIA) and 2D Boolean elements for optic and optoelectronic processors [9-12]. Taking into consideration the above-described approach, consisting in universality, let us recollect some known facts regarding the number of functions [13]. Thus, the search of means aimed at construction of elements, especially universal with programmable tuning, able to perform matrix (multi-valued, continuous) logic operations is very actual problem [10]. One of promising directions of research in this sphere is the application of time-pulse-coded architectures (TPCA), that were considered in works [12-14], these architectures were generalized in work [8]. Besides, the analysis of various algebra logics [8, 14-17] for functional systems allows us to suggest a very useful idea. It is possible to create more sophisticated problem-oriented processors, in which the specific time-pulse operands encoding and only elements of two-valued logic are used, which will realize functions of different logics, continuous etc. The ULE TVL on current mirrors (CM) with photodiodes, current comparators (photocurrents), circuits of limited subtraction (LS), LEDs and drivers is developed in papers [18]. These base elements are used for realization also others elements of continuous logic such as equivalentor (nonequivalentor) and so on [15, 19], but with analog amplitude, and non-time-pulse coding. The optoelectronic photocurrent reconfigurable universal logical element (OPR ULE) on the basis of CL-operation and CM is developed in papers [20-22]. The OPR ULE has sub-pixel configuration of 2x2 elements and consists of 4 photodiodes and 18 transistors. But in that paper not all possible working modes and modifications of the basic cells for the specific applications are considered. It is therefore the purpose of this paper is to demonstrate the possible improvements of such basic cells, hereafter smart multifunctional continuous logic devices (SMCLD), which greatly expand their functionality and the range of tasks.

Design of SMCLD structure. In paper [20] was shown the structural diagram of picture element (PE) for computation of all basic matrix-continuous-logic (MCL) operations in matrix quasi-Boolean algebra $\mathbf{C}=((\mathbf{A}, \mathbf{B}), \boldsymbol{max}, \boldsymbol{min}, -)$ [16, 17]. The PE of matrix TVL (MTVL), performing MTVL operations over matrix temporal functions $\mathbf{O}^{\mathbf{i}}_{\mathbf{t}}(\mathbf{t})$ realize MCLF over continuous logic variables (CLV) $\mathbf{O}^{\mathbf{i}}_{\mathbf{t}}$. The time-pulse coding expanded significantly set of operations [9, 22]. Thus, becomes obvious that for realization TPC SMCLD are necessary PE the TVL by means of which are realized CL-operations over time – pulse signals. The selection of the required MCL-functions performed through the control electric adjusting signals. A circuit diagram of the optical interconnects in sensor systems with MIMO-structure [13], based on the proposed SMCLD, is shown in Fig. 1.

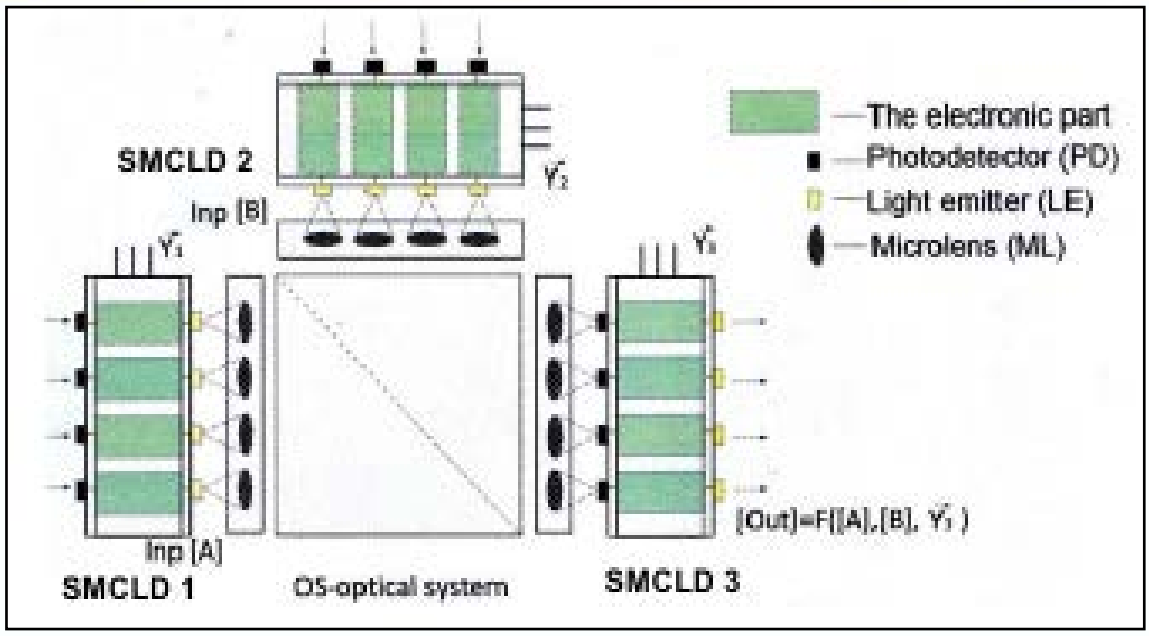


Figure 1. Version of optical interconnect schemes in sensor systems with MIMO-structure based on the proposed design SMCLD with face to face structure.

The use of time-pulse coding (TPC) simplifies the requirement for speed and dynamic range of the photo-detector, as only need to distinguish three levels of amplitude. This significantly increases the noise immunity of such logical transaction devices. For many applications, requires configuring the array of logic elements on various operations in one and the same time. To solve this problem, was proposed one of possible variants [13]. In this paper we consider designing and simulation of the base cell SMCLD, namely its possible minor modifications that significantly extend the functionality and a set of tasks.

Design of SMCLD base cells. Fig. 2 shows the basic structure of the cell SMCLD. It includes a photo-detector (PD), an input selection unit of time-pulse coded signal, a node of synchronization, two identical sample and hold unit (SHU), the analog signal processing unit and an output node with a pulse-width modulator, which are shown accordingly in Figures 3-4. Selection input node, which receives the input photocurrent from the PD, is composed of two CM1 and CM2, four CMOS inverters. Current mirrors act as multiplier of input and reference currents and comparing the input photocurrent current to reference value: 0.5D, 1.5D. CM2 also generates two reference current D 'and D ", are required to operate other components of the cell. Tri-level input TPC signal is a sum of two TPC optical signals from the two previous SMCLD. The signal is separated into two two-level signal with the selection unit. To realize the input selection node, it is required at least 16 transistors, but in this variant we used 20.

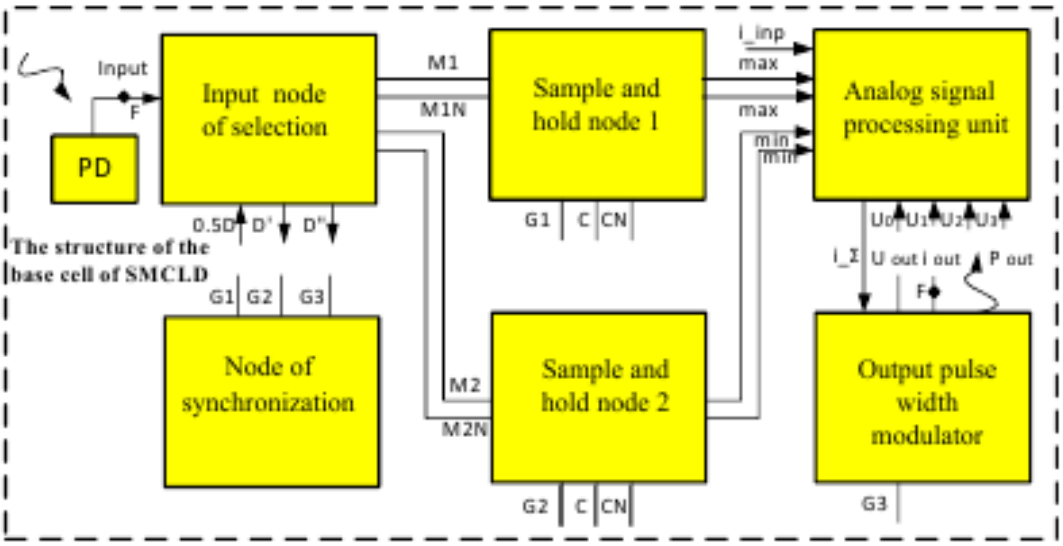


Figure 2. The structure of the base cell of SMCLD

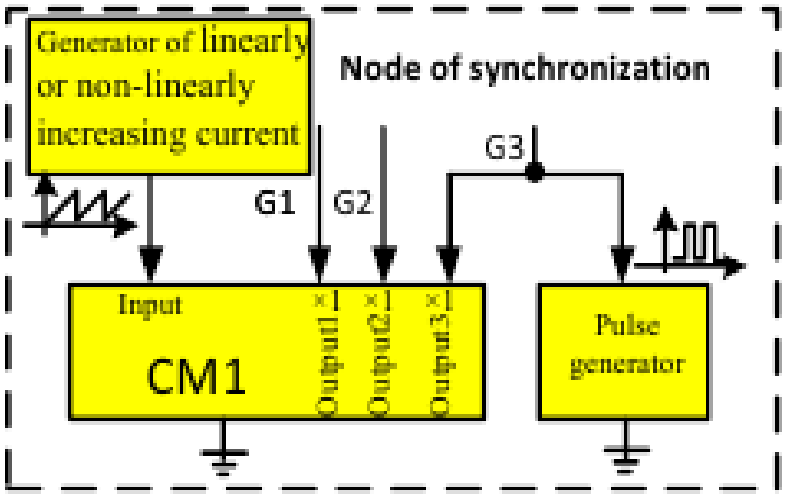


Figure 3. Node of synchronization with generator of linearly or non-linearly increasing current

The node of synchronization as shown in Fig. 3 consists of a mirror which multiplies the saw-tooth rising current or non-linearly. This node can be realized on only 4÷10 transistors. Since these signals are common to all base cells, the node of synchronization can be implemented in other variants, when some generators are outside of the base cell. Each sample and hold unit (SHU) [13] is implemented on 9 CMOS transistors and executes transformation of PWM signal into currents which are proportional to signal duration, storage and reading at requested time using the clock signals C and CN. Figure 4 shows the on the analog signal processing unit, which is realized on 16 CMOS transistors, and which has 4 current inputs, one current output and 4 control inputs. Modification of this node is to use different transmission coefficients K_{nonmax}, K_{min}, K_{neq}, K_{inp} of respective current mirrors

VCCM2, VCCM3, VCCM5, VCCM6. Depending on the control voltages U0÷U3 current output current is formed:

$$i_{\Sigma}=(i_{inp})xK_{inp}xU_0+min(i_x, i_y)xK_{min}xU_1+neq(i_x, i_y)xK_{neq}xU_2+nonmax(i_x, i_y)xK_{nonmax}xU_3.$$

By subtracting from the reference signal D' the signal max, the signal ***nonmax*** is formed. Subtracting the signal ***min*** from the signal ***max***, a signal ***neq*** is generated, which is the non-equivalence of currents. Subtraction circuit is implemented using a limited subtraction on the current mirror. Table 1 shows which function CL is formed at the output of the node at different combinations of control signals U1÷U3, if the control signal U_0=0, if K_{inp}=1, K_{min}=1, K_{neq}=0.5, K_{nonmax}=1.

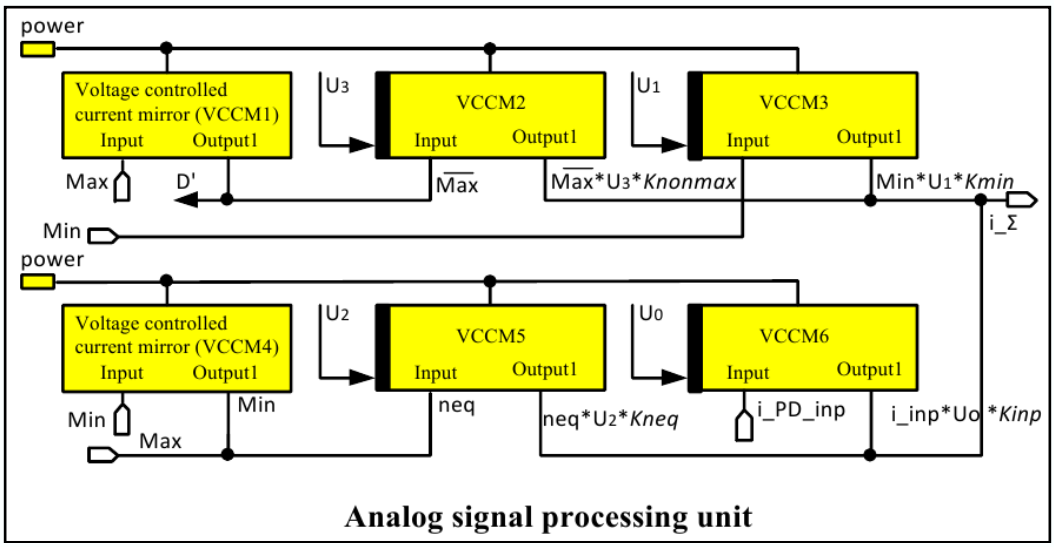


Figure 4. Functional circuit of analog signal processing modified unit

Table 1. Set of CL functions

U_1	U_2	U_3	CL function (i_{Σ})
0	0	0	0
1	0	0	$\min(i_x, i_y)$
0	1	0	$neq(i_x, i_y)*0.5$
0	0	1	$nonmax(i_x, i_y)$
1	1	0	$med(i_x, i_y)$
0	1	1	$nonmed(i_x, i_y)$
1	0	1	$eq(i_x, i_y)$
1	1	1	$D - neq(i_x, i_y)*0.5$

Changing transfer coefficients K_{nonmax}, K_{min}, K_{neq}, K_{inp} current mirrors can create a whole new set of tables, which confirms the significant expansion of functionality and a set of continuously calculated and logical functions. Table 1

shows that changing just one gain K_{neq}, current mirror from 1 to 0,5 we have three new features compared to the set of functions in paper [13]. If you need to select the signal i_{inp} with additional input, such as a photodetector, then U_0=1. Specifying vector of signals U0÷U3, we select one of the required functions of analog processing. Output signals generator node consists of a current comparator with voltage output which is realized on two current mirrors CM1 and CM3 and inverters. Output voltage $\mathbf{U_{out}}$ has the form of a two-level time-pulse coded signal with duration which is set the output variable, is applied to controlled current comparators (CM2 and CM4) with a reference signal D" and produces an output current, and by matching device with light emitter, forms output optical time-pulse coded signal.

Simulation of the modified base cell SMCLD. Initially, we have modeled the basic unit without feedback (point ***F*** in Fig. 2 is absent - no connection) and for $K_{nonmax}=1$, $K_{min}=1$, $K_{neq}=1$, $K_{inp}=1$. The simulation results of this scheme in Fig. 2 on 1.5μm CMOS transistors with OrCAD 16.3 PSpice, for source voltage 3.3V and deferent input signals for Dmax=30μA have shown that the power consumption (without taking into account light emitter and its driver!) of a cell does not exceed 200μW for Dmax=10μA and 1mW for Dmax=20μA, and even for Dmax=30μA peak power (it depends on the duration of the input signals and the generated function) does not exceed 1.5mW. Delay times and pulse fronts are less than 1÷10 nanosecond, and the basic cell is realized on 55÷65 (55 if the mirror current multiplication using only 2 matched transistors) transistors.

The results of other experiments for this operating mode cell are shown in paper [13]. Here we will put only the conclusions from the results. The duration time of pulse-coded signal is in the range of processing cycles, and the pulse repetition period is 12÷120μS. The duration time may be reduced to 1.2μS. This shows that in principle it is possible to increase the frame processing rate to 1MHz, but at the expense of accuracy and complexity of matching photo-detectors with current mirrors. When the amplitude of time-pulse-coded input signals is decreased to Dmax=1μA the power consumption is reduced to 30μW, although the processing period increases to 1.1mS.

From results it is clear, that all continuous-logic functions from the time-pulse coded signals (currents!) are formed correctly: **max, neq, min, nonmax, Dmax, nonmin, eq** (see Fig.5). This experiment shows that it is possible to work in micro-processing mode with frequencies of at 1kHz, arrays up to 100x100 cells, and total consumption of less than 1W. The results [13] of numerous experiments in order to determine errors of output TPC signals showed that the average error for different modes of operation of the basic cells SMCLD does not exceed 5%.

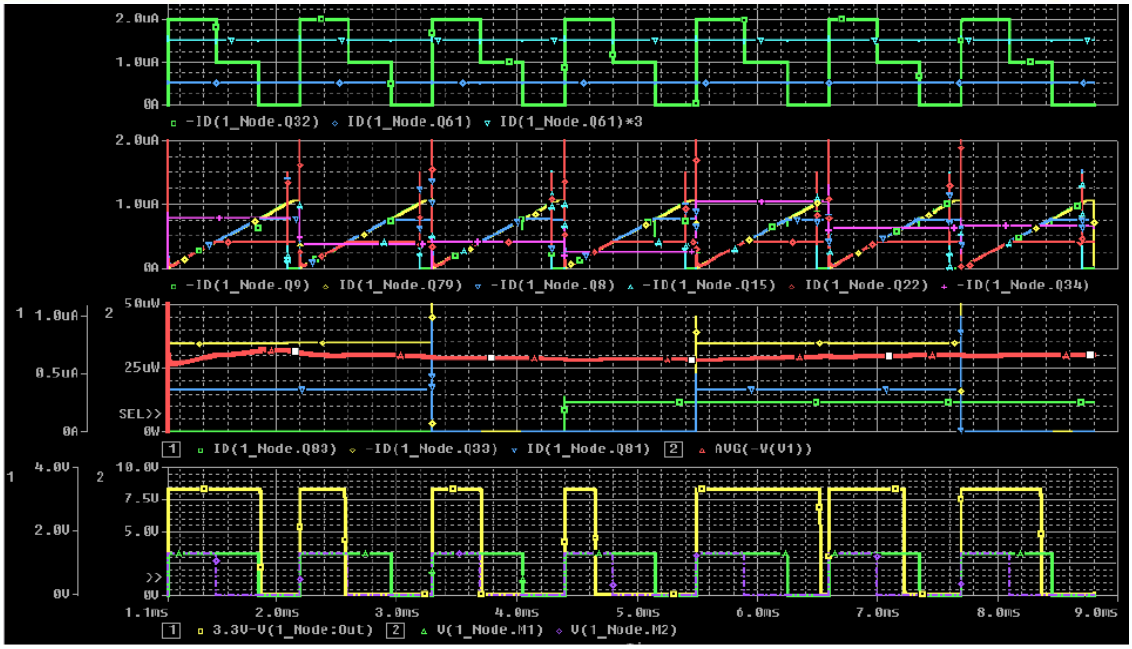


Figure 5. Timing diagram of signals in the base cell for seven (1÷7) conversion periods obtained in the OrCad 16.3 Pspice at 3.3V, **Dmax=1μA**, period is equal to 1.1mS. Duration of the input signal 400μS and 750μS, different operation in different period (sequentially: **max, neq, min, nonmax, Dmax, nonmin, eq**), the output voltage is shown at the bottom right the yellow line.

The simulation results of similar functionality of universal reconfigurable logic devices with dynamic photodiode controls were shown in paper [21]. The significant difference of the proposed cell SMCLD from previously considered in papers [20, 21] is that for all CL functions formed with TPC signals there is start-stop binding for the start of conversion. For some functions in the same papers [20, 21] such binding was not.

The proposed scheme of the base cell can be easily upgraded for processing time-pulse coded input signals pipelining. For this purpose, as shown in Figure 2, by means of the point F the current output is connected to the current input. In this case, when selecting for example function **min** (or whatever) through required number of periods at the output of the base cell SMCLD time-pulse-coded (TPC) signal will be formed with duration equals to the smallest (or **maximum**, **differential**, or otherwise) for the duration of the sequentially received signal at its input.

Within the limitations on the paper size the simulation results of CL-operation in this mode will be presented in the presentation. Figure 6 shows a diagram of the function of forming

$$\mathbf{min}(i_x, i_y) + \mathbf{nonmax}(i_x, i_y) + \mathbf{neq}(i_x, i_y) \times 0.5 = \mathbf{D} - \mathbf{neq}(i_x, i_y) \times 0.5.$$

with a corresponding bottom row of Table 1 vector signals U0÷U3 for the case of input variables to the duration 0,5μS и 9,5μS. The output signal is, as expected, is approximately equal to 5,5 μS.

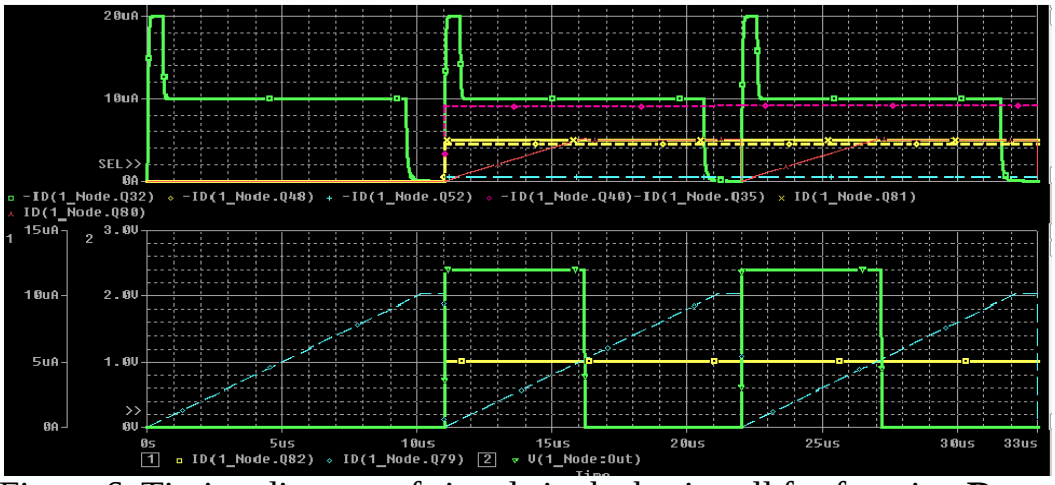


Figure 6. Timing diagram of signals in the basic cell for function **D-neq(i_x, i_y) x 0,5**. In the lower diagram the green line shows the TPC output signal, yellow line corresponding analog current, and blue linearly increasing current synchronization.

Enhancing the functionality of modified cell SMCLD possibly through the use of nonlinear transformations in the PWM output node. The simulation results in this mode are shown in Figure 7. Let us explain the simulation result shown on Figure 7 the left. Length of the input signals respectively 6μS and 8μS, the analog output signal, as shown by the yellow line in the lower diagram is 7μA (it corresponds to the time interval 7μS, determined by the intersection point of the yellow and purple lines), and the output time interval after the nonlinear transformation is approximately 8,5μS and formed by the blue line. Let us explain the simulation result shown on Figure 7 the right. Length of the input signals respectively 1μS and 3μS, and the output time interval after the nonlinear transformation is approximately 4,5μS, not 2μS. In addition, non-linear transformations can be carried out in SHN1 and SHN2 using nonlinear rising currents G1 and G2 node of synchronization. Figure 8 shows the results of simulations.

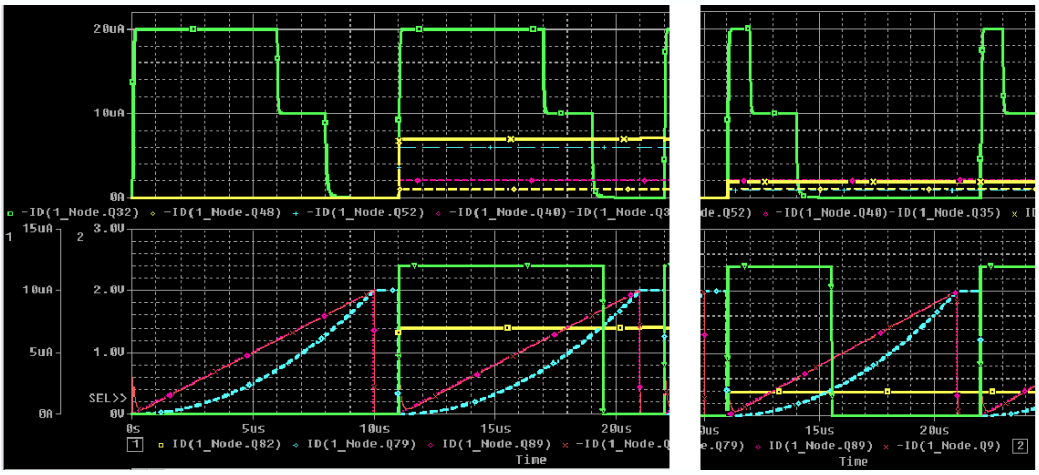


Figure 7. Timing diagram of signals in the basic cell for function **med(i_x, i_y)** and subsequent nonlinear processing on the output node.

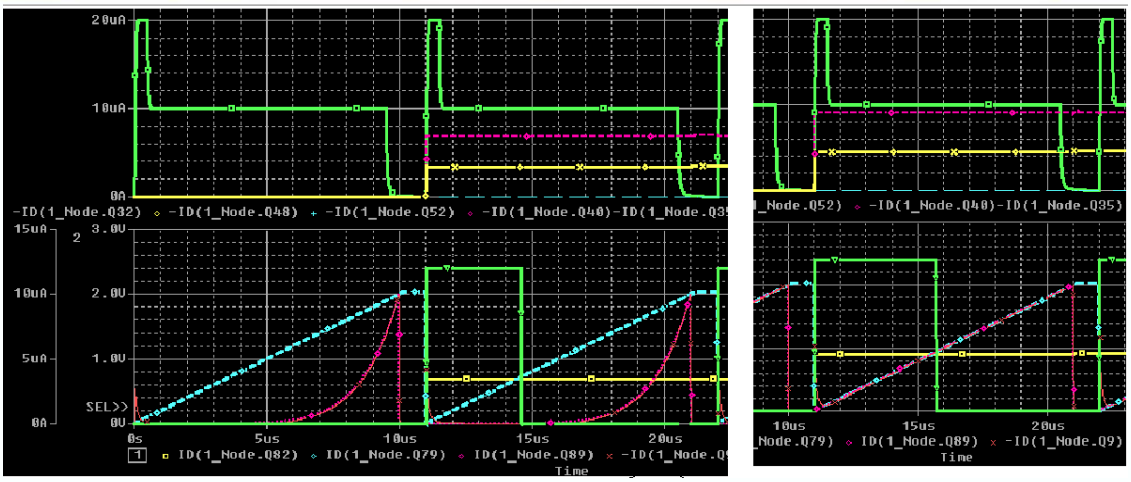


Figure 8. Timing diagram of signals in the basic cell for function **neq(i_x, i_y) x 0,5** and subsequent nonlinear processing on the output node.

Let us explain the simulation result shown on Figure 8 the left. Length of the input signals are respectively 0,5μS and 9,5μS, the analog output signal, as shown by the yellow line at the bottom of the chart (it corresponds to the output time interval 3,5μS, determined by the intersection point of the yellow and blue lines). Let us explain the simulation result shown on Figure 8 the right. Timing diagram of signals in the basic cell with linear processing and SHN and the output node. Length of the input signals are respectively 0,5μS and 9,5μS, and the output time interval is approximately 4,7μS. Changing nonlinearity coefficients of nonlinear functions of increasing currents and shape of the curves can be selected conversion functions required input or output signals. Analyzing the dependencies described by the formulas above and shown in Table. 1, the results obtained and presented here of the simulation of the main modes of operation of the developed devices, we can conclude that the use of nonlinear transformations with the use of special nodal synchronization functions significantly expands the range of functions performed. In this case, complex nonlinear functions are implemented that have several arguments and allow you to easily control the selection of the required function, its parameters and options. If we add a small analog processor block described in articles [23, 24] and consisting of only two dozen transistors, it is easy to implement analog-to-digital conversion of photocurrents, corresponding to binary or Gray code. And based on the approach and circuit solutions proposed here, it is possible to develop and create a whole range of new devices, hardware accelerators, processors and self-learning convolutional-like neural structures of the so-called equivalent paradigm [25 - 28]. Since the photocurrent of our cell considered here is input and output for processing in a time interval, then, in our opinion, a simpler option for implementing analog-to-digital conversion and activation nodes that implement controlled arbitrary nonlinear transformations is to use the approach that was proposed in article [7]. These modifications will be considered in our next work.

Conclusions. We have proposed a new approach for designing and modeling of SMCLD implementations as advanced basic cells of high-performance sensor systems with MIMO structure. Such SMCLDs implement the function of continuous logic with current inputs and current outputs based on CMOS circuits. We have developed several simple modifications and improvements of one basic version of one channel SMCLD. The concept of building a basic SMCLD cell is to use current mirrors implemented on 1.5 μm CMOS transistors. The presence of 55÷65 transistors, 1 photodiode and 1 LED makes the proposed circuits quite compact and allows their integration into 1D and 2D arrays. We have considered aspects of expanding the functionality of the proposed circuits, shown the results of their modeling and possible prospects for the application of these circuits, in particular, for time-pulse coding for multi-valued, continuous and matrix logics. The results of modeling the min, max, equivalence (EQ) functions and others, such as: ***neq(ix, iy)x0.5, med(ix, iy)***, as well as nonlinear transformations of various types, showed that the level of logical variables can vary from 1 μA to 10 μA for low-power variants.

The advantage of the proposed approach and the developed SMCLD is a significant expansion of the set and types of functions and functional transformations, including nonlinear transformations with different parameters, a simple circuit change of the transmission-reflection coefficients in current mirrors and a change in the functional time dependences of current synchronization. The basic SMCLD cells have low power consumption <1 mW and a processing time of about 1÷11 μs at a supply voltage of 2.4÷3.3 V. It is confirmed that the entire set of possible functions will be implemented using such an SMCLD by simple code-controlled tuning. Such basic cells, integrated into a 32x32 array, allow achieving a performance of 10^12 CL-logical operations/sec.

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